4046B
MICROPOWER PHASE-LOCKED LOOP

DESCRIPTION – The 4046B is a Micropower Phase-Locked Loop consisting of a low power linear Voltage-Controlled Oscillator, a Source Follower Circuit, two different Phase Comparators, and a Zener diode. The Voltage-Controlled Oscillator has two External Capacitor connections (C_{exta}, C_{extb}), two External Resistor connections (R_{exta}, R_{extb}), a Voltage-Controlled Oscillator Input (I_{VCO}) and a Voltage-Controlled Oscillator Output (O_{VCO}). The Source Follower Circuit provides a Demodulated Output (O_D) from the Voltage-Controlled Oscillator. An active LOW Enable Input ($\overline{E}$) common to both the Voltage-Controlled Oscillator and the Source Follower Circuit is also provided. Phase Comparator I and Phase Comparator II have common Signal (I_S) and Comparator (I_C) Inputs and separate outputs; Phase Comparator I Output (O_{PCI}), Phase Comparator II Output (O_{PCII}), and Phase Pulse Output (O_{PII}). An input to the Zener diode (I_Z) is also provided.

The Voltage-Controlled Oscillator requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. A second external resistor (R_2) may be used to allow frequency offset. External resistor R_3 and external capacitor C_2 combined serve as a low pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). Output O_D is provided to avoid loading the low pass filter. External resistor R_4 is required if this output is utilized. O_D must be left open when not utilized. The output from the Voltage-Controlled Oscillator (O_{VCO}) may be connected directly or indirectly through CMOS frequency dividers (i.e., the 4018B, 4020B, 4022B, 4024B, 4029B, 4040B, 4518B, 4520B, 40160B, 40161B, 40162B, 40163B, 40192B or 40193B) to the Comparator Input (I_C). With the Enable Input (E) HIGH both the Voltage-Controlled Oscillator and the Source Follower Circuit are OFF to minimize power consumption. With $\overline{E}$ LOW, both are enabled.

For direct-coupling between O_{VCO} and I_C, the voltage swing at the Voltage-Controlled Oscillator Output (O_{VCO}) must be within standard CMOS logic levels ($V_{OH} \geq 0.7 \times V_{DD}$ and $V_{OL} \leq 0.3 \times V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the Signal Input (I_S).

Phase Comparator I is an Exclusive OR circuit ($I_C \oplus I_S$). I_C and I_S must have 50% duty cycles to maximize lock range. When the Output of Phase Comparator I (O_{PCI}) is connected back to the Voltage-Controlled Oscillator through the low pass filter network, an averaged voltage to I_{VCO} forces oscillation at a center frequency.

Phase Comparator II is an edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output. Phase Comparator II triggers on LOW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. The Output of Phase Comparator II (O_{PCII}) provides voltage levels and duty cycles corresponding to frequency and phase differentials between I_C and I_S. When O_{PCII} is connected to the Voltage-Controlled Oscillator Input (I_{VCO}) through the low pass filter network, a corresponding voltage across capacitor C_2 is adjusted until the Signal (I_S) and Comparator (I_C) Inputs are equal in both frequency and phase. At this point Phase Comparator II maintains a constant voltage across Capacitor C_2. When this stability has been established, the Phase Pulse Output (O_{PII}) is HIGH indicating a locked condition. Power dissipation in the low pass filter is reduced when Phase Comparator II is used.

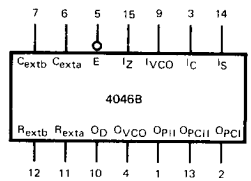
A zener diode is provided for regulating the power supply voltage, if necessary.

- **VERY LOW POWER CONSUMTPION**
- **HIGH VCO LINEARITY, 1% TYPICAL**
- **CHOICE OF 2-PHASE COMPARATORS**
- **ENABLE INPUT (ACTIVE LOW) FOR LOW POWER DISSIPATION IN STANDBY MODE**
- **ON-CHIP ZENER DIODE FOR SUPPLY REGULATION**
- **VCO FREQUENCY DRIFT WITH TEMPERATURE = 0.04% / °C TYPICAL AT V_{DD} = 10 V**

PIN NAMES

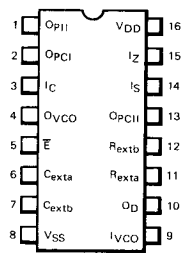
I_Z	Zener Diode Input
I_S	Signal Input
I_C	Comparator Input
I_{VCO}	Voltage-Controlled Oscillator Input
$\overline{E}$	Enable Input (Active LOW)
C_{exta}, C_{extb}	External Capacitor Connections
R_{exta}, R_{extb}	External Resistor Connections
O_{PCI}	Phase Comparator I Output
O_{PCII}	Phase Comparator II Output
O_{PII}	Phase Pulse Output
O_D	Demodulator Output
O_{VCO}	Voltage-Controlled Oscillator Output

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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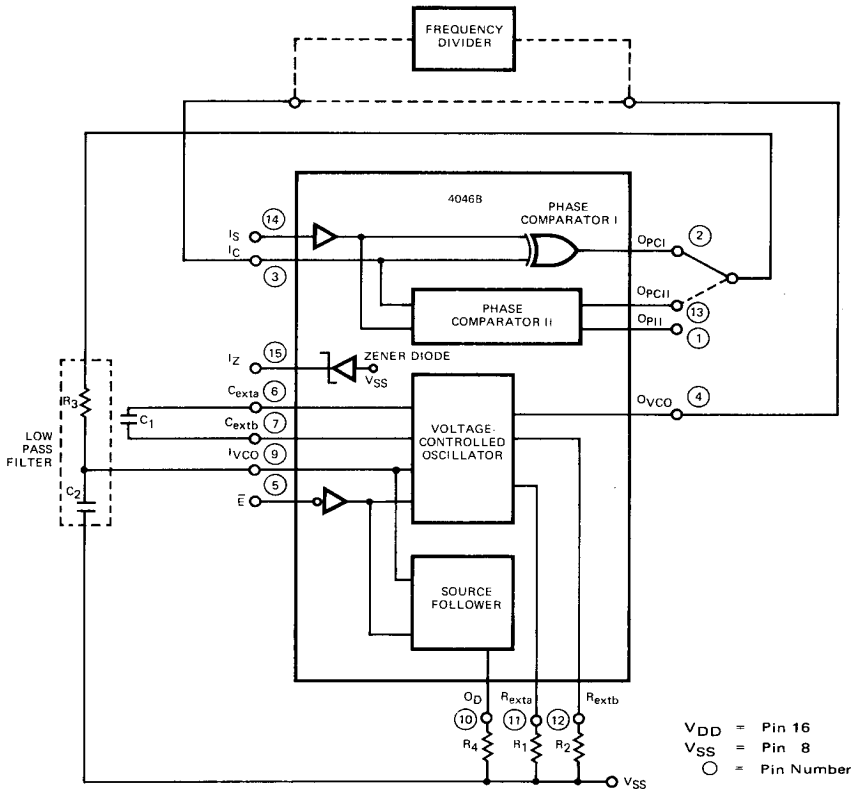
BLOCK DIAGRAM



$10\ k\Omega \leqslant R_1 \leqslant 1\ M\Omega$
$10\ k\Omega \leqslant R_2 \leqslant 1\ M\Omega$
$10\ k\Omega \leqslant R_4 \leqslant 1\ M\Omega$
$C_1 \geqslant 100$ pF at $V_{DD} = 5$ V
$C_1 \geqslant 50$ pF at $V_{DD} = 10$ V

FUNCTIONAL DESCRIPTION – The 4046B, Micropower Phase-Locked Loop consists of a low power linear Voltage-Controlled Oscillator (VCO), a Source Follower circuit (SF), two Phase Comparators (PCI and PCII) and a Zener diode.

VOLTAGE-CONTROLLED OSCILLATOR

The VCO requires one external capacitor (C_1) and one external resistor (R_1) to determine operational frequency range. External resistor R_2 is used to allow for frequency offset, if required. It is recommended that R_1 and R_2 have a value between 10 kΩ and 1 MΩ. At V_{DD} = 5 V, C_1 should be greater than or equal to 100 pF, and at V_{DD} = 10 V, C_1 should be greater than or equal to 50 pF.

External resistor R_3 and external capacitor C_2 combined serve as a low-pass filter to the Voltage-Controlled Oscillator Input (I_{VCO}). The user is allowed a wide range of resistor-to-capacitor ratios for R_3 and C_2 because of the high imput impedance at I_{VCO} (approximately 10^{12} Ω).

To avoid loading of the low-pass filter, the Demodulator Output (O_D) should be connected through external resistor R_4 as shown in the Block Diagram. It is recommended that R_4 have a value between 10 kΩ and 1 MΩ. If the O_D output is not utilized it must be left open.

The Voltage-Controlled Oscillator Output (O_{VCO}) provides a 0.3 V_{DD} to 0.7 V_{DD} output voltage swing and may be connected to the Comparator Input (I_C). O_{VCO} may, also be connected indirectly to I_C via CMOS frequency dividers (i.e., the 4018B, 4022B, 4029B, 4040B, 4518B, 4520B, 40160B, 40161B, 40162B, 40163B, 40192B, and 40193B.)

An Enable Input ($\overline{E}$) to the VCO and SF is provided for minimum stand-by power dissipation. With the $\overline{E}$ Input HIGH both the VCO and the SF are OFF. With $\overline{E}$ LOW, both are enabled.

PHASE COMPARATORS

For direct-coupling between O_{VCO} and I_C, the voltage swing at O_{VCO} must be within standard CMOS logic levels ($V_{OH} \geq 0.7\ V_{DD}$ and $V_{OL} \leq 0.3\ V_{DD}$); otherwise the signal from O_{VCO} must be capacitively coupled to the self-biasing amplifier at the I_S Input.

Phase Comparator I is an Exclusive OR circuit ($I_C \oplus I_S$). For maximum lock range, inputs to I_C and I_S must have 50% duty cycles. (Lock range, $2f_L$, is defined as that frequency range of input signals upon which the 4046B will stay locked from an initial locked condition). With no signal or noise input, Phase Comparator I provides an average output voltage equal to $V_{DD}/2$ at the O_{PCI} Output. This average output voltage is supplied to the I_{VCO} Input through the low-pass filter, which in turn forces the VCO to oscillate at a center frequency (f_O).

Capture range $2f_C$, is defined as that frequency range of input signals upon which the 4046B will lock from an initial unlocked condition. Capture range for PCI is directly dependent upon the characteristics of the low-pass filter network and may be as great as the lock range. Thus, PCI allows the user a phase-locked loop system which will remain in a locked condition despite high amounts of noise in the input signal.

It should be noted that with the use of PCI the system may lock onto input signals with frequencies that are near harmonics to the center frequency of the VCO. It should further be noted that the phase angle between the I_C and I_S Inputs will vary between 0° and 180°. At the center frequency the phase angle is 90°. *Figure 2* illustrates a typical Phase Angle versus Average Output Voltage response characteristic for PCI. *Figure 3* illustrates the typical waveforms for a phase-locked loop system employing PCI and locked at a center frequency.

Phase Comparator II is edge-triggered digital memory network with four flip-flop stages, associated control circuitry and a 3-state output, controlled internally. PCII triggers on LOW-to-HIGH transitions at the Signal (I_S) and Comparator (I_C) Inputs and is independent of duty cycle at these inputs. If the input frequency at I_S is higher than the input frequency at I_C, the p-channel output transistor at O_{PCII} is turned "ON" continuously, pulling the output (O_{PCII}) toward V_{DD}. If the input frequency at I_C is higher than the input frequency at I_S, the n-channel output transistor at O_{PCII} is turned "ON" continuously, pulling the output toward V_{SS}. If the input frequencies at I_S and I_C are equal, but I_S lags I_C in phase, the n-channel output transistor is turned "ON" for a period of time corresponding to the phase difference. If the input frequencies at I_S and I_C are equal, but I_C lags I_S in phase, the p-channel output transistor is turned "ON" for a period of time corresponding to the phase difference. Thus, over a period of time the voltage at capacitor C_2 is adjusted until the I_C and I_S input signals are of the same frequency and phase. Once this stability is reached, both p- and n-channel output transistors at O_{PCII} are "OFF". O_{PCII} becomes an open circuit holding the voltage across C_2 constant.

Once this stability is attained, the Phase Pulse Output (O_{PII}) is HIGH indicating a locked condition.

With PCII no phase difference is present between I_C and I_S over the entire VCO frequency range. Furthermore, since the 3-state Phase Comparator II Output (O_{PCII}) is mostly in the "OFF" condition, power dissipation through the low-pass filter is minimized. It should also be noted that $2f_C = 2f_L$ independent of the filter network in a phase-locked loop utilizing PCII. *Figure 4* shows typical waveforms for a phase-locked loop system employing Phase Comparator II and locked at a center frequency.

Fig. 2 CHARACTERISTICS OF PHASE COMPARATOR I AT THE LOW PASS FILTER OUTPUT.

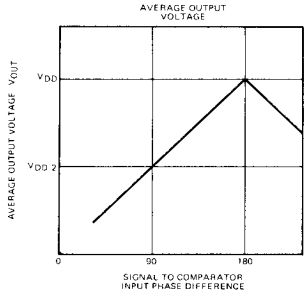


Fig. 3 A PLL SYSTEM USING PHASE COMPARATOR I.

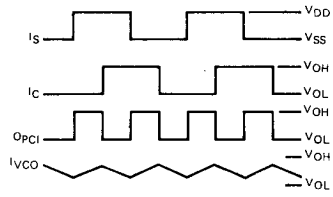


Fig. 4 A PLL SYSTEM USING PHASE COMPARATOR II

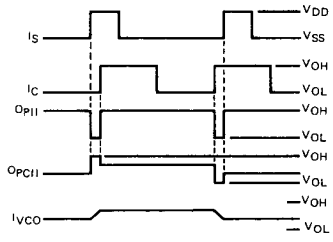


Fig. 5 TYPICAL LOW-PASS FILTERS.

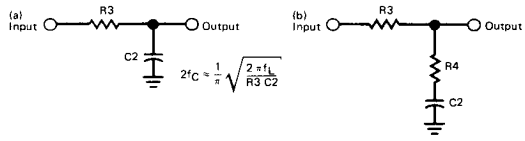
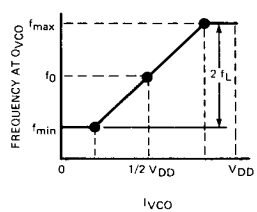


Fig. 6 DESIGN INFORMATION.

Characteristic	Using Phase Comparator 1	Using Phase Comparator 2
No signal on input I_S	VCO in PLL system adjusts to center frequency (f_0).	VCO in PLL system adjusts to minimum frequency (f_{min}).
Phase angle between I_S and I_C	90° at center frequency (f_0), approaching 0° and 180° at ends of lock range ($2f_L$).	Always 0° in lock (positive rising edges).
Locks on harmonics of center frequency.	Yes	No
Signal input noise rejection.	HIGH	LOW
Lock frequency range (2fL).	The frequency range of the input signal on which the loop will stay locked if it was initially in lock. $2f_L$ = full VCO frequency range = $f_{max} - f_{min}$.	
Capture frequency range ($2f_C$).	The frequency range of the input signal on which the loop will lock if it was initially out of lock.	
	Depends on low-pass filter characteristics (Figure 5) $f_C \leq f_L$	$f_C = f_L$
Center frequency (f_0).	The frequency of O_{VCO} when $I_{VCO} = 1/2\ V_{DD}$	
O_{VCO} freqency (f).	$f \approx \frac{K\left[\frac{I_{VCO}-1.65}{R_1} + \frac{V_{DD}-1.35}{R_2}\right]}{(C_1+32)(V_{DD}+1.6)}$ MHz (at 25°C)	
NOTE: The information presented here is meant only as a design guide.	where: V_{DD} in V; 5 V ≤ V_{DD} ≤ 15 V I_{VCO} in V; 1.65 V ≤ I_{VCO} ≤ (V_{DD} −1.35 V) R_1 and R_2 in MΩ; R_1, R_2 ≥ 0.005 MΩ C_1 in pF; C_1 ≥ 50 pF K = 0.95 @ V_{DD} = 5 V = 0.95 @ V_{DD} = 10 V = 1.08 @ V_{DD} = 15 V	

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (Note 1)

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEMP	TEST CONDITIONS
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

ELECTRICAL CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C

SYMBOL	PARAMETER		LIMITS V_{DD} = 5 V MIN	TYP	MAX	V_{DD} = 10 V MIN	TYP	MAX	V_{DD} = 15 V MIN	TYP	MAX	UNITS	TEST CONDITIONS
t_{TLH} t_{THL}	Propagation Delay, Output Transition Time			72 72			48 48			38 38		ns	C_L = 50 pF R_L = 200 kΩ Input Transition Times ⩽ 20 ns
PHASE COMPARATORS													
R_{IN}	Input Resistance	I_S		200			400			700		MΩ	
		I_C		10^6			10^6			10^6			
V_{IN}	AC Coupled Input Sensitivity for I_S			200			400			700		mV p-p	
	DC Coupled Input Sensitivity for I_S, I_C		See Note 1 for V_{IH} and V_{IL} Characteristics										
VOLTAGE CONTROLLED OSCILLATER													
	Temperature-Frequency Stability			0.12 0.24			0.04 0.08			0.015 0.03		%/°C	No Frequency Offset, f_{min} = 0 See Note 3
				0.06 0.12			0.05 0.10			0.03 0.06			Frequency Offset, $f_{min} \neq 0$ See Note 4
	Linearity			1			1			1		%	See Note 2
	Output Duty Cycle			50			50			50		%	O_{VCO} tied to I_C
R_{IN}	Input Resistance to I_{VCO}			10^6			10^6			10^6		MΩ	
f_{max}	Maximum Operating Frequency			0.9			1.7			2.3		MHz	See Note 6
SOURCE FOLLOWER													
V_D	Offset Voltage at O_D			1.65			1.65			1.65		V	R_4 > 10 kΩ
	Linearity			0.1			0.6			0.8		%	See Note 5
ZENER DIODE													
V_Z	Zener Voltage			7			7			7		V	I_Z = 50 μA
R_Z	Zener Dynamic Resistance			100			100			100		Ω	I_Z = 1 mA

Notes:
1. Additional dc characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. I_{VCO} = 2.5 V ± 0.3 V, R_1 > 10 kΩ for V_{DD} = 5 V. I_{VCO} = 5 V ± 2.5 V, R_1 > 400 kΩ for V_{DD} = 10 V. I_{VCO} = 7.5 V ± 5 V, R_1 > 1 MΩ for V_{DD} = 15 V.
3. $R_2 = \infty$, %/°C ∝ 1/(f−V_{DD}).
4. %/°C ∝ 1/(f−V_{DD}).
5. R_4 > 50 kΩ, I_{VCO} = 2.5 V ± 0.3 V for V_{DD} = 5 V. I_{VCO} = 5 V ± 2.5 V for V_{DD} = 10 V, I_{VCO} = 7.5 V ± 5 V for V_{DD} = 15 V.
6. R_1 = 5 kΩ, $R_2 = \infty$, I_{VCO} = V_{DD}, C_1 = 50 pF.