ROHDE & SCHWARZ

Manual

MOBILE TESTER SMFP2

332.0015.53

Printed in West Germany

VOLUME I

Manual consists of 2 volumes

R 43412 - 1

Table of Contents Page

Table of Contents

Table of Contents

Table of Contents

MOBILE TESTERS SMFS2 AND SMFP2

NEW TECHNICAL FEATURES AND ADDITIONAL DATA

Spectral purity of RF signal generator	Phase noise improved by 6-10 dB to -126 dBc/Hz typ. (20 kHz from carrier).
Reference oscillator	temperature-controlled crystal oscillator as standard equipment for improved accuracy of RF signal generator frequency and frequency meter.
Long term	$<\pm 5 \cdot 10^{-8}$/month
Temperature effect	$<\pm 1 \cdot 10^{-7}$ over nominal-temperature range after 15 min warm up.
2-tone modulation	using additional internal RC generator (1 kHz or 400 Hz) for simultaneous generation of test and pilot-tone modulation.
	Independent setting of modulation sources: 400 Hz / 1 kHz as 2nd source and RC generator (SMFS2) or AF synthesizer (SMFP2, optional for SMFS2) as 1st source. Sources may be interchanged.
Modulation of 2nd source	setting range / resolution
AM	0 to 100% / 0.1%
FM	0 to 10 kHz / 10 Hz
φM	0 to 1 rad / 0.001 rad
Accuracy	as for single-tone AM/FM/φM modulation + resolution. For the maximum permissible sum modulation (tone 1 + tone 2) refer to data sheet.
Deviation meter	in addition to automatic switchover, the detector can now be locked to peak or rms weighting.
Selective call coder additional settings	(optional for SMFS2) repeat tone as 1st tone alarm tone as 1st or last tone CCIR standard with 70 ms tone length 1st tone length 450 ms or 750 ms
Additional standards	EEA, EIA, Euro Customer defined frequencies.

095.7489-0581

S/N, SINAD meter — integration of 150 measurements for steady display

Memory facilities — battery-supported non-volatile memory with additional capacity for 6 complete instrument settings.

Option Adjacent-Channel Power Meter SMFP-B61

Improved adjacent-channel power meter with increased measurement range.

Measurement limit f <519 MHz — better than -72 dB (typ. -76 to -80 dB)
f >519 MHz — better than -68 dB (typ. -72 to -76 dB)

Refer to data sheet, option SMFP-B6, for further data.

Option Duplex Deviation Meter SMFP-B91

Independent deviation meter for SMFS2 and SMFP2 for measurements on repeater stations and full-duplex radios. For integration in instruments with Analog Display SMFS-B9.

Frequency range — 10 to 1000 MHz

Further data as in data sheet.

Option Duplex Deviation Meter SMFP-B41

Independent deviation meter as add-on for SMFS2 and SMFP2.

Data as option SMFP-91.

Summary of options available for SMFS2 and SMFP2.

Option		SMFP2	SMFS2	Order No.
1 GHz Frequency Extension	SMFP-B2	x	x	332.9706.50
60-W Power Meter	SMFP2 B3	x	x	357.8610.02
Control Interface	SMFS-B5	o	x	332.9106.02
AF Synth./Selective-Call Coder	SMFS2 B7	o	x	346.6810.02
Selective-call Decoder	SMFS2 B6	x	x 1)	346.7000.02
RF Millivoltmeter	SMFS2 B8	x	x	332.9306.02
Analog Display	SMFS B9	x	x	346.5008.02
Adjacent-channel Power Meter	SMFP B61	x 2)	x 2)	395.7217.02
Duplex Deviation Meter	SMFP B41	x 2)	x 2)	372.1412.02
Duplex Deviation Meter	SMFP B91	x 3)	x 3)	372.0016.02

o = standard   x = may be fitted as option

For further data, accessories, recommended extras and ordering information refer to data sheets 332 001 and 332 002.

This Technical Information applies only to SMFS2 and SMFP2 with serial Nos. from 872 508/001

1) only together with SMFS B7

2) add-on, ex-factory fitting only

3) only together with SMFS-B9; ex-factory fitting only

Supplement
to
SMFP2 Manual
332.7790

Page 2.22 Add to section 2.3.3.3.1:

With the setting

| Ø | | MOD |

the modulation display is not changed. The OVERFLOW LED lights.

For Ø modulation the modulation must be switched off (better S/N ratio).

Supplement

to

SMFP2 Manual

322.7790

Page 2.5	Ref. 20 4th line: delete "frequency and".
Page 2.6	Ref. 28: change "20A" to "10A".
Page 2.9	Under fivetone modulation: interchange "switch-on" and "switch-off".
Page 2.17	Add to section 2.3.1: At every new switch-on, the main function - transmitter measurement - is set. The generator settings selected before switch-off are maintained. Twotone modulation is switched off. The Basic state can be recalled with 99 REF; all REF functions are thereby erased.
Page 2.18	Section 2.3.3.1.1: change "1040 MHz" to "1000 MHz".
Page 2.23	Add to section 2.3.3.3.2: For external modulation the pilot-tone modulation must be switched off with 2000 REF.
Page 2.46	Section 2.5.4 3rd line from below: change "BR12" to "BR3".
Page 3.13	Section 3.2.2.19.2 1st line: change "700 mV" to "1500 mV" change "10 mW = 10 dBm" to "50 mW = 17 dBm".

Page 5.10 — Lowest case:
change "B6" to "B24";
change "B7, B8, B9" to "B25, B26, B27";
change "B17" to "B15".

Page 5.12 — Lowest case:
change "T20" to "T4".

Page 5.59 — Change para "Adjustment of A/D converter B6" as follows:

Adjustment of A/D converter B24

- Apply TTL H level to initiative conversion line.
- Connect BR3 to ground terminal.
- Adjust R50 so that pins 3 to 11 (B24) are at TTL L level, and pin 12 (B24) just changes from TTL H to TTL L level (do not turn any further).
- Apply 10.22 V to BR3.
- Adjust R46 so that pins 3 to 11 (B24) are at TTL H level and pin 12 (B24) at TTL L level.

The modulation processing circuit does not require adjustment.

2. Preparation for Use and Operating Instructions

2.1 Legend for Figs.2-3 and 2-4

The values given in the following section are not guaranteed values. Only the specifications given in the data sheet are binding.

Ref. No.	Labelling	Function
1	HF · RF FREQUENZ MHz	8-digit display of RF frequency set or measured, in MHz.
2	- ΔF kHz + ΔF kHz	Keys for varying the frequency of the RF signal generator by defined amounts and for setting the channel spacing of the adjacent-channel power meter. The numerical values are entered in kHz via keyboard 25. When entering standard channel step sizes the following types of internal modulation are automatically set. 12.5 kHz FM 1.5 kHz deviation 20 kHz FM 2.8 kHz deviation 25 kHz FM 3.0 kHz deviation 30 kHz FM 3.0 kHz deviation
3	SIGN. GEN.	Transfer key. After pressing this key, the signal generator is set to the frequency entered viy keyboard 25. This frequency is immediately available at RF level output 48 and is displayed in MHz on 1. As soon as the frequency is displayed on 1 the transfer key lights up. If the key is pressed without having entered a numerical value via keyboard 25, the RF frequency meter is switched off and the previous frequency setting is read out.

Ref. No.	Labelling	Function
4	+6 dB	Pressing this key increases the RF level at output 48 by +6 dB. The next time the key is pressed the previous level is reset. When the level is increased the key lights up.
5	HF · RF PEGEL/LEVEL µV, mV, dBm, dBµV, W, µW, dB	3 1/2-digit display of output level or input power or voltage at RF millivoltmeter or adjacent-channel power.
6	µV, mV, dBm, dBµV	Transfer keys. Pressing one of these keys resets the RF level at output 48 previously selected viy keyboard 25, the physical unit corresponding to the labelling of the key pressed. If one of the other three keys is subsequently pressed without entering other data via keyboard 25 the level is converted to the newly selected physical unit and displayed on 5. Since the attenuator is set in 0.1-dB steps, display 5 read out the dB values set and not the values entered in mV or µV.
7	HF/RF OFF	Key for switching off the RF signal. When the RF signal is switched off, the key lights up. Display 5 reads out 000 without physical unit.
8	MOD. INT.	Key for transfer of modulation depth, frequency or phase deviation after being entered via keyboard 25. Type of modulation must have already been selected by means of 50. Physical unit for entering data: FM in kHz φM in rad AM in % The key 8 lights up when internal modulation is switched on. The modulation is switched off if the key is pressed again without entering other data via keyboard 25. If this key is pressed when the modulation is switched off and without having entered other data via keyboard 25, the previously entered value is set again and the modulation measurement is discontinued .

Ref. No.	Labelling	Function
9	HF · RF MODULATION (kHz, rad, %, INT.)	3-digit display of the set or measured value of FM (kHz), AM (%) or φM (rad).
10	MOD. EXT.	Key for input of the modulation (%, Δf or rad) after entering numerical value via keyboard 25. The voltage at input socket 39 must be 1 V_{rms}. The type of modulation can be selected by means of keys 11. Key 10 lights up when external modulation is switched on. If this key is pressed when the modulation is switched off and without having entered other data via keyboard 25 the previously entered value is set again and the modulation measurement discontinued.
11	FM, φM, AM	Key for selecting type of modulation in the case of external modulation. The key pressed lights up even if external modulation is switched off. The numerical values of the modulation (%, Δf or rad) are entered via keyboard 25 and transferred by pressing the key 10 MOD. EXT.
12	FEST - FIXED FREQ. ⇨ ⇦	Key for selection of the fixed audio frequencies. Each time the left-hand key is pressed, the next higher value is selected. Each time the right-hand key is pressed, the next lower value is selected. The selected frequency is displayed on 13.
13	NF · AUDIO FREQUENZ kHz, Hz	4-digit display of set or measured AF frequency.
14	MOD. GEN.	Key for input of AF level after entering the value in mV via keyboard 25. The AF signal is then available at output 34. As soon as the output level is displayed on 16, key 14 lights up. If this key is pressed without having entered a numerical value on keyboard 25, the previous output voltage setting is read out and the AF or DC measurement discontinued.

Ref. No.	Labelling	Function
15	EXT. NF/AC	Key for connecting the AF voltmeter to the input socket 31. The key lights up when the voltage applied to socket 31 is displayed on 16.
16	NF · AUDIO PEGEL/LEVEL mV, V, A, DC	4-digit display of the AF output level, the AF voltage input to socket 31 or the DC voltage or current input to sockets 28.
17	CCITT	Key for switching CCITT AF filter on or off. The key lights up when the filter is switched on.
18	KLIRRFAKTOR DISTORTION ON ⇕ f	By pressing the ON key the filter and AF generator are set to 1 kHz. Cyclic switching key for test frequencies 1 kHz, 300 Hz, 500 Hz of distortion meter. The AF generator is automatically set to the test frequency. The setting is displayed on 13. By pressing the ON key again the measurement is discontinued.
19	SINAD	Key for switching on the SINAD meter. If no numerical value has been entered via keyboard 25 the SINAD value at the particular RF level setting is indicated. The AF is set to 1 kHz. This value is displayed on 13. After the numerical value in dB has been entered the RF level is automatically adjusted so as to obtain the selected SINAD ratio. The RF level is displayed on 5 and the SINAD ratio on 20. During the SINAD ratio measurement simultaneous quasi-analog display of the units digit is provided on 20. By pressing the key again, the SINAD mode is turned off. Key 19 lights up when the SINAD meter is switched on.

Ref. No.	Labelling	Function
20	RESULT %, dB	3-digit display of result of distortion, SINAD and S/N measurements. The circular quasi-analog display makes setups easier. It can be assigned to the frequency and level meters (RF and AF), the modulation-depth meter as well as the DC ammeter and voltmeter by meany of the two cursor keys 22. The digit defined by the cursor location is used to drive the circular quasi-analog display by pressing key 1 on keyboard 25 and the REF. key 29.
21	S/N	Key for switching on the S/N meter. The S/N ratio of the transmitter or the receiver section can be measured by pressing key 49 or key 51 respectively. Measurement of S/N ratio of transmitter section: If no data have been entered via keyboard 25 the S/N ratio of the demodulated transmitter signal is measured and displayed on 20. Measurement of S/N ratio of receiver section: If no data have been entered via keyboard 25 the S/N ratio of the signal available at socket 31 (NF · AC METER) is measured at the given modulation and displayed on 20. If a numerical value has been entered in dB, the RF level is automatically adjusted so as to obtain the selected S/N ratio. The RF level is displayed on 5 and the S/N ratio on 20. During the S/N ratio measurement simultaneous quasi-analog display of the units digit is provided on 20. By pressing the key again the measurement is discontinued. Key 21 lights up when the S/N meter is switched on.

Ref. No.	Labelling	Function
22	+ ⇐ ⇒ −	Variation and cursor keys. The two keys ⇐ and ⇒ shift the cursor one digit further to the left or to the right. The + and the - keys vary the output setting digit marked by the cursor. If the key is pressed momentarily, the value is varied in individual steps. If the key is held down, the value is varied continuously.
23	OVERFLOW	LED for indication of an illegal entry or of an illegal measured value.
24	REMOTE	LED which lights up if the Tester is remote controlled via the IEC bus.
25	7 8 9 4 5 6 1 2 3 0 . - C STO RCL	Keyboard for entry of numerical values. C cancels the entry. STO together with 0, 1 or 2 stores the RF frequency setting in MHz; STO together with 3, 4 or 5 stores variation of this frequency in kHz. RCL together with 0, 1, 2, 3, 4 or 5 recalls the stored value. Example: Entry: 123.45 SIGN. GEN. (key 3) STO 0 (RF in MHz) 4800 STO 3 (variation in kHz) Recall: RCL 0 (RF in MHz) RCL 3 (+variation in kHz) RCL-3 (-variation) STO 90 to 95 stores full front-panel setup. RCL 90 to 95 recalls the stored setups.
26	LOCAL	Key which is pressed to return to manual operation.
27	NETZ POWER	AC supply and battery switch.
28	U_{DC} I_{DC} < 30 V < 20 A < 200 mA	Input sockets for DC voltage and current measurements.

29 REF Prior to pressing this key the function is to be called by numerical entry on keyboard 25.

Transmitter

		Keys	LED
	Modulation sensitivity (automatic setting of nominal deviation of test item in transmitter measurement mode)	2 REF	
	Reset selective call decoder	1 0 REF	
	Read, reset selective call decoder	1 1 REF	
*)	Transfer of measured transmitter frequency for receiver measurement		
	Simplex	1 0 1 REF	1
	Duplex, receiver in lower band	1 0 2 REF	1
	Duplex, receiver in upper band	1 0 3 REF	1
	Switching off	1 0 0 REF	0
	(With duplex units the duplex band spacing in kHz must be stored with STO 3.		
*)	Acknowledgement signal on	1 0 5 REF 0 REF	1
	See 2.3.4.7 off	1 0 6 REF	0
*)	Adj.-channel power without channel limit	1 1 7 REF 0 REF	1
	See 2.3.4.9 with channel limit	1 1 8 REF	0
	RF measuring diode off (prevents RF distorsions at 30-dB output)	1 2 0 REF 0 REF	1
	RF measuring diode on See 2.3.4.2	1 2 1 REF	0
	Modulation measurement peak only	1 2 6 REF 0 REF	1
	rms only	1 2 7 REF 0 REF	1
	normal	1 2 5 REF	0
	Selective call decoder base 1 (B10)	1 9 8 REF	
	base 2 (B20)	1 9 9 REF	

LED keys: 0 = switching LED off (The LED is not switched off until all functions that have caused it to be on are off.)
1 = switching LED on.

*) See page 2.11

		Keys	LED
Indication of RF variation — on off Indication of RF frequency variation up to ±99,9 kHz referred to current RF frequency setting. Indication on AF frequency display.	on: [1] [0] [7] [REF] off: [1] [0] [8] [REF]	[0] [REF]	1 0
*) Bandwidth measurement — without centre-freq. error with centre-freq. error Indication on AF frequency display Indication of centre-frequency error on RF frequency display.	without centre-freq. error: [1] [1] [5] [REF] with centre-freq. error: [1] [1] [6] [REF]	[0] [REF] [0] [REF]	1/0 1/0
*) Quieting Measurement of RF sensitivity for 20 dB noise suppression. The RF level is indicated on 5 PEGEL/LEVEL, the noise suppression on 20 RESULT. Note on bandwidth and quieting measurements: Prior to calling up the bandwidth test routines, enter nominal RF frequency and, if necessary, modulation frequency in the kHz range. Upon completion of the measurement the device functions are disabled and, by entering [0] via the keyboard and pressing the [REF] keys SIGN.GEN. and the MOD.GEN., the displays of centre-frequency error and bandwidth must be erased after reading off the measured values.	[1] [1] [9] [REF]		
Squelch sensitivity See 2.3.4.10	[1] [2] [9] [REF]	[0] [REF]	0
Changeover of AF generator 2 — 400 Hz 1000 Hz See 2.3.3.3.4	400 Hz: [2] [0] [0] [REF] 1000 Hz: [2] [0] [1] [REF]		
AF source for doubletone modulation — AF Gen 2 AF Gen See 2.3.3.3.4	AF Gen 2: [2] [0] [2] [REF] AF Gen: [2] [0] [3] [REF]		
Setting the modulation value of the AF of the second modulation — 2000+mod. value FM: 1000 = 10.00 kHz ΦM: 1000 = 1.000 rad AM: 1000 = 100.0 % Exemple: 2.4 kHz FM deviation [2] [2] [4] [0] [REF]	[2] [0] [0] [0] [REF] to [3] [0] [0] [0] [REF]		

LED keys: 0 = switching LED off (The LED is not switched off until all functions that have caused it to be on are off.)
1 = switching LED on.

*) See page 2.11

Other functions:

			Keys LED
Switching off the functions identified with 0 REF	0 REF		0
Cursor	1 REF		
Reinitialization of complete set	9 9 REF		
Setting the BCD outputs via BU 401 Second figure = 1st decade Third figure = 2nd decade Fourth figure = 3rd decade	1 0 0 0 REF 1 9 9 9 REF		

Transmitter and receiver

Average over 15 measurements 50 for SINAD, S/N 150 bandwidth	3 REF 4 REF 1 4 REF		
Taking into account external attenuator Example: 5run 5 REF 3.2 W/dBm for 3.2 dB attenuator See 2.3.4.2	5 REF		
Fivetone modulation switch on Fivetone modulation switch off	6 REF 7 REF		0 1
Selective call standard ZVEI1 (coder/decoder Selective call standard CCIR (coder/decoder	8 REF 9 REF		
RF millivoltmeter 0-dB probe 20-dB probe 40-dB probe	1 7 REF 1 8 REF 1 9 REF	 0 REF 0 REF	0 1 1
Switching of relays via BU 402 First figure = relay number Second figure = 0 = open relay 1 = close relay	2 0/1 REF 3 0/1 REF 4 0/1 REF		

LED Keys: 0 = switching LED off (The LED is not switched off until all functions that have caused it to be on are off.)

1 = switching LED on.

	Keys		Keys LED
Switching of relays via BU 402 (cont.)	[5] [0/1] [REF] [6] [0/1] [REF] [7] [0/1] [REF] [8] [0/1] [REF] [9] [0/1] [REF]		
Frequency response indication off	[1] [1] [0] [REF]		0
AF: Reference value: current measured value	[1] [1] [1] [REF]	[0] [REF]	1
AF: Reference value: AF level setting	[1] [1] [2] [REF]	[0] [REF]	1
*) Mod.: Reference value: current measured value	[1] [1] [3] [REF]	[0] [REF]	1
*) Mod.: Reference value: Modulation level setting	[1] [1] [4] [REF]	[0] [REF]	1
Indication of 111 to 114 on result display in dB.			
Rejection filter for AF and modulation measurement — switch on	[1] [2] [2] [REF]	[0] [REF]	1
switch off	[1] [2] [3] [REF]		0
Frequency selectable with 300 Hz, 500 Hz, 1 kHz			
Selective call standard for coder — #) ZVEI1	[1] [8] [0] [REF]		0
#) coder/decoder — #) ZVEI2	[1] [8] [1] [REF]		0
#) CCIR	[1] [8] [2] [REF]		0
#) CCIR70	[1] [8] [3] [REF]		0
EEA	[1] [8] [4] [REF]		0
EIA	[1] [8] [5] [REF]		0
EURO	[1] [8] [6] [REF]		0
Special code (for entry see 300)	[1] [8] [7] [REF]		0
Selective call coder — normal	[1] [9] [0] [REF]		
First tone — 700 ms	[1] [9] [1] [REF]		1
First tone — 450 ms	[1] [9] [2] [REF]		1

LED keys: 0 = switching LED off (The LED is not switched off until all functions that have caused it to be on are off.)
1 = switching LED on.

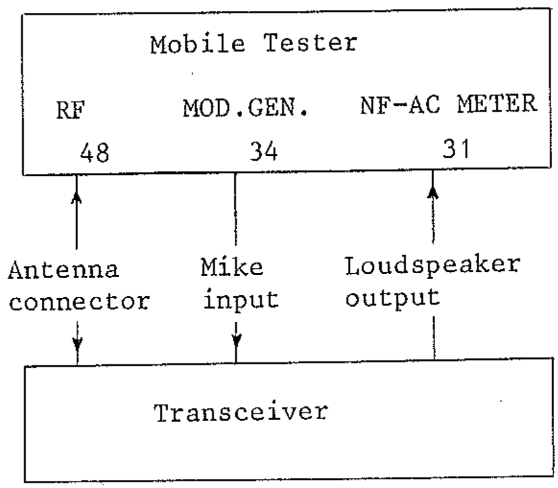
*) See page 2.11

				Keys LED
Selective call coder	normal	[1] [9] [3] [REF]		0
Repeat tone	at first place	[1] [9] [4] [REF]		1
Emergency tone	at first place	[1] [9] [5] [REF]		1
Emergency tone	at last place	[1] [9] [6] [REF]		1
Use of AF frequency setting as selective call code for special tone sequence	Code 0	[3] [0] [0] [REF]		0
	Code 1	[3] [0] [1] [REF]		0
	Code 2	[3] [0] [2] [REF]		0
	Code 3	[3] [0] [3] [REF]		0
	Code 4	[3] [0] [4] [REF]		0
	Code 5	[3] [0] [5] [REF]		0
	Code 6	[3] [0] [6] [REF]		0
	Code 7	[3] [0] [7] [REF]		0
	Code 8	[3] [0] [8] [REF]		0
	Code 9	[3] [0] [9] [REF]		0
Repeat tone		[3] [1] [0] [REF]		0
Emergency tone		[3] [1] [1] [REF]		0
Tone length for special tone sequence	70 ms	[3] [2] [0] [REF]		0
	100 ms	[3] [2] [1] [REF]		0
	40 ms	[3] [2] [2] [REF]		0
	33 ms	[3] [2] [3] [REF]		0

LED keys: 0 = switching LED off
(The LED is not switchd off until all functions that have caused it to be on are off.)
1 = switching LED on.

*) Prior to calling up these functions make sure that a radio set in perfect working order is connected according to the drawing, otherwise the automatic measuring procedure might never come to an end and consequently no (or a useless) result might appear on the display.

Test setup:



Ref. No.	Labelling	Function
30	U/I DC	Key for DC voltage and current measurements. The test items are connected to input sockets 28.
31	NF-AC METER 1 mV - 10 V	Input socket for AF voltage and frequency measurements. Press key 15 to connect the AF voltmeter to input socket 31 and key 33 to connect the frequency counter to input socket 31.
32	+20 dB	Key for increasing the AF generator output level at socket 34 by 20 dB. If the level is increased, the key lights up. If the key is pressed again, the original level is set again.
33	EXT. NF/AC	Key for connecting the AF frequency meter to input socket 31 for external frequency measurement. The measured AF frequency is displayed on 13.
34	MOD. GEN.	Output socket of the AF generator.
35	BEAT FREQ.	Key for measuring the beat frequency between the RF frequency set and the RF signal applied to the socket FREQ. METER 47. The result is displayed on 13. The modulation is switched off.
36	DEMOD. FREQ.	Key for measuring the audio frequency of a demodulated RF signal applied to input socket 48.
37	DEMOD. SIGN. $R_i \approx 50\ \Omega$	Output socket for the demodulated signal
38	MOD. GEN.	Key for setting the frequency of the AF generator after entering the desired frequency via keyboard 25.
39	MOD. EXT. 1 V_{rms} $R_i = 600\ \Omega$	Input socket for external modulation signals. For input voltages required see sections 2.3.3.3.2 and 2.3.3.3.3.
40	$- \frac{PK + PK}{2} +$	Keys for switching on the modulation meter. The "-" key measures the negative and the "+" key the positive peak value. The $\frac{PK + PK}{2}$ measures the mean value of the modulation. The key selected lights up.
40.1	HF-RF PROBE	Socket for connection of RF probe or insertion unit for Option SMFS2B8.
41	PROBE	Key for switching on RF Millivoltmeter SMFS2B8, if provided. The voltage is displayed in V or dBm on 5. By pressing the key again, the display is changed over from V to dBm, or vice versa.
42	ON OFF	Potentiometer for adjusting the volume for the headphones connected to socket 44 or the internal loudspeaker; also on/off switch for the internal loudspeaker.

Ref. No.	Labelling	Function
43	NKL dBμW	Key for switching on the adjacent-channel power meter (if option SMFP-B6 is fitted). The power is displayed on <u>5</u> in dB relative to the input power (lower key) or in μW (upper key).
44	$R_i \approx 2$ kΩ	Headphones socket
45	W/dBm	Key for switching on the power meter. The power is displayed in W or dBm on <u>5</u>. By pressing the key again, the display is changed over from W to dBm, or vice versa.
46	FREQ. MET.	Key for connecting the frequency meter to RF input socket <u>47</u>
47	FREQ. METER R_i = 50 Ω 10 mV - 1 V	Input socket for the frequency meter
48	HF · RF R_i = 50 Ω	Socket for connecting the radio-telephone set. RF output from the signal generator and RF input to the test facilities.
49	SEND. TR.	This key must be pressed for transmitter measurements.
50	FM φM AM	Keys for selecting the type of modulation.
51	EMPF. REC.	This key must be pressed for receiver measurements.
52		Air filter.
53	IEC 625 BUS	IEC-bus connector.
54	HF · RF 30 dB	RF socket to which the signal applied to socket <u>48</u> is brought out after attenuation by 30 dB.

Ref. No.	Labelling	Function
55	ADDRESS	10-way switch for setting the IEC-bus address.
56	NF · AF 1 kHz	Output socket for a 1-kHz AF signal with a 1.7-V output level.
57	BU402	15-way output socket which can be controlled via the IEC bus.
58	REF. 10 MHz	Input socket for an external 10-MHz reference signal.
59	BU401	15-way output socket which can be controlled via the IEC bus.
60	47 - 420 Hz	AC supply connector.
61	M1C M2E	Power fuse.
62	200 - 255 V 105 - 135 V	Voltage selector.
63	BATT. T16A	Battery fuse.
64	+ 11-33 V -	Battery terminals.

2.2 Preparation for Use

The Mobile Tester SMFP2 can be powered from the mains or from a battery.

AC supply operation is possible in two voltage ranges, from 105 to 135 V and from 200 to 255 V. The Tester is factory-adjusted for operation over the voltage range from 200 to 255 V. For adaptation to the voltage range 105 to 135 V, change over the voltage selector 62 (Fig. 2-4) and exchange the power fuse.

Fuses required:	105 to 135 V	M2E DIN 41571
	200 to 255 V	M1C DIN 41571.

Spare fuses are supplied with the Tester.

A voltage between 11 V and 33 V is required for battery operation. The battery is connected to terminals 64. The battery input is protected against wrong polarity and fused with a 16-A fuse DIN 41571. The fuse is screwed into fuse holder 63. A spare fuse is supplied with the Tester.

The Mobile Tester SMFP2 has the basic width of a 19" unit. A rack adapter (332.7978.02) is required for mounting it in a 19" rack. To do so, remove the screws on either side, and take off the panels and the side strips as well as the carrying handle. There are holes provided for screwing down the rack adapter. The RF socket cannot be moved to the rear panel.

2.3 Operating Instructions

The operator controls the SMFP2 by pressing keys, with the exception of the volume control for which a potentiometer is used.

The digital displays and the keys are logically organized in horizontal and vertical sections (Fig. 2-1).

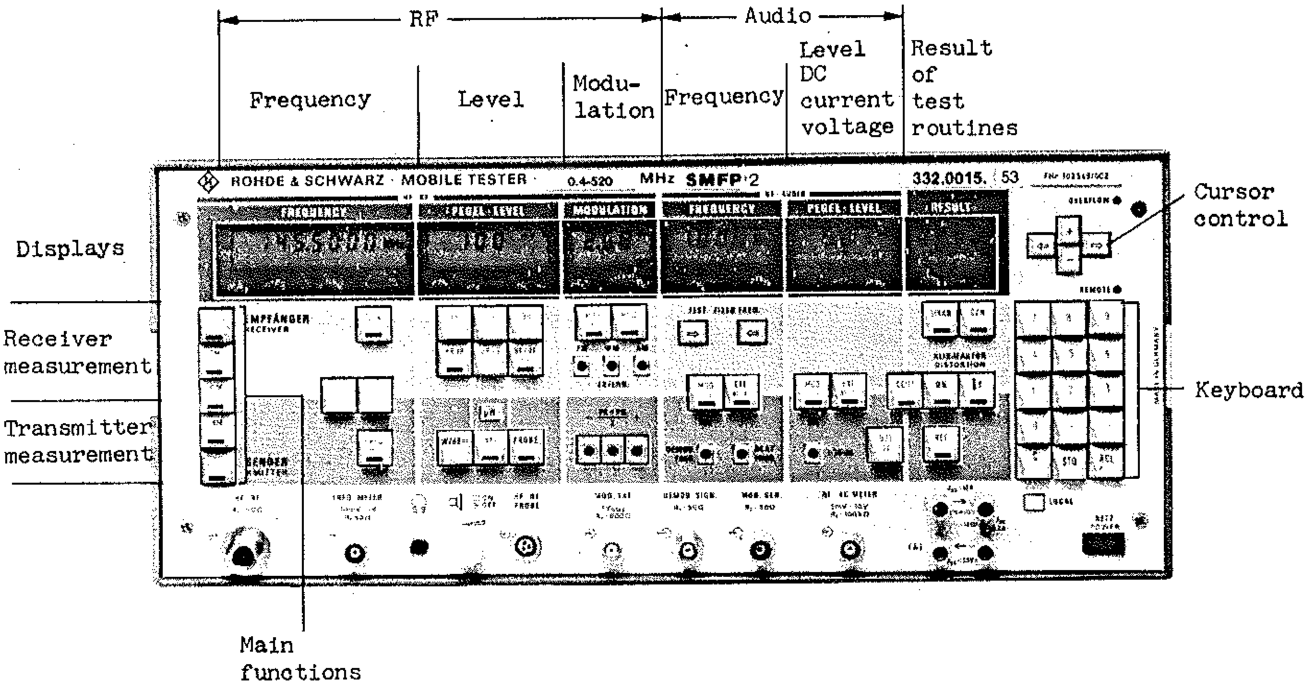


Fig. 2-1 Organization of the front panel

All data to be set must first be entered via keyboard 25 (Fig. 2-3). Then by pressing a key in the section assigned to the desired function the entered value is transferred and the physical unit defined at the same time.

Illegal settings are not accepted. If, for example, an RF frequency above or below the frequency range of the Tester is entered, the LED 23 OVERFLOW lights. The same is true for the other functions. The LED signals that the last entry cannot be transferred or that the test value is not within the measurement range. If, subsequently, an admissible value or instruction is entered, or if the key C is pressed on keyboard 25 the LED goes off.

2.3.1 Switch-on State

The SMFP2 is switched on by pressing key 27 (Fig. 2-3). At switch-on the Tester assumes the following defined basic state:

Main function: transmitter measurement "FM".

Display 20 simultaneously reads out the program version, e.g. P 0.

The RF signal frequency is 100 MHz. The frequency deviation is 2.8 kHz and the modulation frequency is 1 kHz.

The RF level is 1 µV.

The settings can be displayed by pressing key 51 EMPF. REC.

The AF output level is set to 1 mV.

2.3.2 Basic Setting

The keys 49 XMITTER and 51 RECEIVER (Fig. 2-3) allow selecting transmitter or receiver measurement, respectively. The type of modulation is selected by means of the three keys 50 FM, φM and AM.

If an input power of > 0.5 W is applied to socket 48 RF the Tester switches automatically over from receiver measurement to transmitter measurement.

2.3.3 Receiver Measurement

If the key 51 RECEIVER (Fig. 2-3) is pressed the receiver measurement mode is selected, with an RF signal being output to the test item via socket 48 RF. In addition, the AF level meter is switched on.

2.3.3.1 Setting and Varying RF Frequency (Carrier)

Setting the RF frequency

To set the RF frequency, first enter the desired numerical value in MHz via keyboard 25 (Fig. 2-3). Zeros behind the decimal point at the end of a figure need not be filled in. For example, "423" can be entered for 423.000 MHz or "423.2" for 423.20.

After the RF value has been entered press key 3 SIGN. GEN.. This defines that the value entered is an RF frequency in MHz and sets the signal generator immediately to this frequency. The RF frequency is displayed on 1.

Varying the RF frequency

A frequency entered via the keyboard 25 can be varied either in decade steps or in steps of any selected size:

For variation in decade steps set the cursor (marker on the display) to the digit which is to be varied by means of the keys 22 ⟸ ⟹. The frequency is varied by pressing either of the keys 22 "+" or "-".

The frequency can be switched using any desired channel spacing by entering the numerical value of the desired step size in kHz via the keyboard 25 and subsequently pressing one of the two keys 2 "- ΔF" or "+ ΔF". The step size entered is stored and the frequency can be increased or decreased by the stored value as often as desired by repeatedly pressing one of the keys 2. Any frequency step can be entered, from 0.1 kHz to the maximum step size, the entire frequency range. Just make sure that the entry is always in kHz.

If the frequency range is exceeded by decade frequency variation or variation in channel steps, LED 23 OVERFLOW lights indicating that the last command cannot be executed; e.g. it is not possible to increase 515 MHz by a step of 10 MHz. If then, however, the frequency is varied by, say, +1 MHz, the overflow indication goes off and the frequency is increased by 1 MHz. The overflow indication can also be turned off by pressing key "C" on keyboard 25.

2.3.3.1.1 Setting and Varying the Frequency Using the 1-GHz-Frequency Extension SMFP-B2

If the Tester is fitted with the Option SMFP-B2 the frequency range is extended to 1040 MHz, and the overflow indication 23 (Fig. 2-3) lights up only if this value is exceeded.

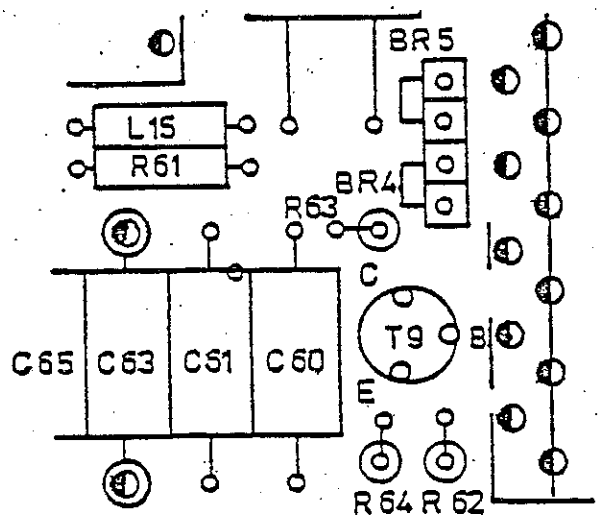
The frequency is set and varied in the same way as described in section 2.3.3.1.

The resolution of the indication is 200 Hz over the frequency range 520 to 1040 MHz. If the frequency is entered via the keyboard, if it is varied in decade steps or steps of any size the frequency setting is rounded to the nearest 200 Hz.

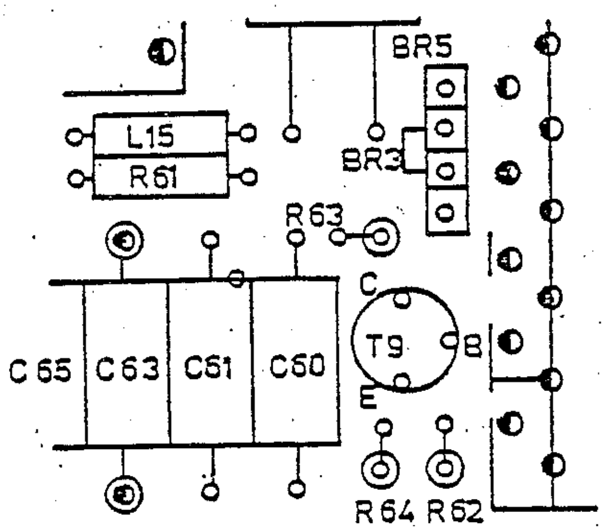
2.3.3.1.2 Reference Frequency

The signal generator contains an internal 10-MHz crystal reference oscillator from which the output frequency is derived using a synthesizer circuit. A TTL output at the reference frequency is available at BNC socket 58 REF. 10 MHz (Fig. 2-4) for external control purposes. The signal generator can, however, also be supplied with an external reference frequency of 10 MHz, if, for example, it is to be driven from another unit or from a central standard frequency. To this end, it must be internally modified. After this conversion the socket 58 REF. 10 MHz is used as an input for the external reference frequency. A sinewave signal of 10 MHz and 0.5 V will do; a TTL level can also be applied.

The Tester is supplied with BNC socket 58 REF. 10 MHz wired as an output. To convert the socket to serve as a reference frequency input, a link on reference board 302.6215 must be changed. To do so, first remove the bottom cover after loosening the screws on either side, and then lift off the lid of the large shielding box. The location of the circuit board 302.6215 is shown on the lid. After unplugging the circuit board the plug-in contacts at the lower right-hand edge are accessible and the link can be changed as required in accordance with Fig. 2-2.



a) Reference frequency output



b) Reference frequency input

Fig. 2-2 Location of the plug-in link

If the reference board is fitted with the option SMS-B1 (temperature-controlled reference oscillator) the option must be removed if an external reference frequency is to be applied.

2.3.3.2 Setting and Varying the RF Output Level

Setting the RF output level

To set the RF output level first enter the desired value in either µV, mV, dBµV or dBm via keyboard 25 (Fig. 2-3). In the case of negative dBµV and dBm values enter a minus sign ("-" key) before the numerical value. Zeros behind the decimal point at the end of a figure need not be entered.

After entering the level value press key 6 µV, mV, dBµV or dBm corresponding to the physical unit of the value entered previously. This defines firstly that the value entered is for an output level or output voltage and immediately sets the level or voltage at output 48 RF. The level or voltage is displayed together with the physical unit on 5 LEVEL.

Since the attenuator is set in 0.1-dB steps, display 5 reads out the dB values set and not the values entered in mV or µV.

Permissible level or voltage range:

Unmodulated, FM and φM	AM
0.03 µV to 1000 mV	0.03 µV to 500 mV
-30 dBµV to +120 dBµV	-30 dBµV to +114 dBµV
-137 dBm to +13 dBm	-137 dBm to +7 dBm

If another physical unit key 6 is pressed after the level has been set without a new numerical value being entered via keyboard 25, the level setting is converted into the new physical unit and displayed on 5.

Varying the RF output level

An output level entered via keyboard 25 can be varied in decade steps. To do so, adjust the cursor to the digit on display 5 that is to be varied using the keys 22 ⟸ ⟹. By pressing one of the two keys 22 "+" or "-" momentarily, the level is increased or decreased by one unit of the selected decade. If the key is held down the level is varied continuously, first slowly and after three steps in a fast sequence.

If the level is varied beyond the limits of the range of adjustment the LED 23 OVERFLOW lights up.

Continuous, electronically controlled fine variation of the level down to -10 dB is possible by means of key 22 "-" if the cursor is adjusted to the extreme right digit of the level displayed on 5. This does not interrupt the signal at output 48. The approximate value of the fine variation is indicated by a vertical marker row on display 5. In addition, the numerical value displayed on 5 is always correct, changing with the fine variation.

If fine variation exceeds the -10-dB limit the attenuator switches over and fine variation starts again with 0 dB and so does the marker indication on display 5. The level at output 48 is cut off for the short period of time the attenuator switches over. Starting from this setting fine variation is now again possible continuously down to -10 dB and without the signal being interrupted.

2.3.3.2.1 Physical Units of Level Indication

All the values entered via keyboard 25 (Fig. 2-3) and the output levels displayed on 5 are valid for voltage or power with a resistance termination of 50 Ω. In all cases the actual output voltage is indicated. The EMF is double the value.

The physical unit dBμV is a logarithmic measure of the output voltage relative to 1 μV. With an output voltage V_{out} (V)

$$V\ (\text{dB}\mu\text{V}) = 20 \log \frac{V_{out}\ (\text{V})}{1\ \mu\text{V}} .$$

Hence, an output voltage of exactly 1 μV corresponds to 0 dBμV. If the voltage is greater than 1 μV a positive dBμV value is obtained and if the voltage is smaller than 1 μV a negative dBμV value is obtained.

The unit dBm defines the output power that would be dissipated in a resistive termination, as a logarithmic measure relative to 1 mW. With a power P (W)

$$P\ (\text{dBm}) = 10 \log \frac{P\ (\text{W})}{1\ \text{mW}}$$

or with a voltage V_{out} (V)

$$P\ (\text{dBm}) = 10 \log \frac{V_{out}^2\ (\text{V})}{50 \times 1\ \text{mW}} .$$

If the test item or load is not 50 Ω the effective power is reduced by reflection.

Hence, depending on the VSWR the output power

$$P_{(load)} = P_{(indication)} \frac{4 \times \text{VSWR}}{(1 + \text{VSWR})^2} .$$

2.3.3.2.2 Level with Amplitude Modulation

If the amplitude modulation is switched on the maximum output level is reduced by 6 dB. The LED 23 OVERFLOW (Fig. 2-3) lights up as soon as 500 mV or 7 dBm or 114 dBμV are exceeded when entering or varying the output level. Settings above this level limit are not possible. If a higher level is set in unmodulated operation and amplitude modulation is switched on only afterwards, 23 OVERFLOW lights up and the amplitude modulation is not activated.

There is no level reduction for level settings below this limit. The level entered and displayed with amplitude modulation is the mean value of the carrier.

2.3.3.2.3 Output Cut-off

The RF signal at output 48 can be switched off by means of key 7 HF/RF OFF (Fig. 2-3) without affecting the frequency, modulation or level setting. Key 7 lights up when the signal is cut off. Display 5 reads out 000 without unit. The RF signal reappears at output 48 if key 7 is pressed again.

2.3.3.3 Setting the Modulation

2.3.3.3.1 Internal Modulation

For internal modulation the built-in AF generator is used as a modulation generator and the desired modulation frequency is entered according to section 2.3.3.4.

First select the type of modulation by means of keys 50 FM, φM or AM (Fig. 2-3). The key pressed lights up.

Next select the numerical value for the modulation depth in %, the frequency deviation in kHz or the phase deviation in rad via keyboard 25. The zeros behind the decimal point at the end of the numerical value entered need not be filled up.

The numerical value entered is transferred by pressing key 8 MOD. INT., immediately set, and read out on the 3-digit display 9. The key 8 is lit during internal modulation. By pressing the key again the modulation is switched off. The entries remain, however , stored and the same modulation is obtained as before when the key is pressed again.

The resolution of the setting and display depends on the value entered:

for amplitude modulation

with m = 0 to 9.95 %	....	0.05 %
m = 10 to 99 %	....	0.5 %;

for frequency modulation

with Δf = 0 to 9.95 kHz	....	0.05 kHz
Δf = 10 to 99.5 kHz	....	0.5 kHz
Δf = 100 to 125 kHz	....	1 kHz;

for phase modulation

with $\Delta f/f_{mod}$ = 0 to 5 rad	....	0.05 rad.

If the values entered are in still smaller steps the SMFP2 rounds off automatically to the next value.

2.3.3.3.2 External Modulation

An external modulation signal can be applied to socket 39 MOD. EXT. (Fig. 2-3).

First select the type of modulation by means of keys 11 FM, φM or AM EXTERN. The key pressed lights up.

If the modulation voltage at socket 39 is exactly 1 V the desired numerical value entered via keyboard 25 for the modulation depth in %, the frequency deviation in kHz or the phase deviation in rad is correctly transferred, set and displayed on 9 as soon as key 10 MOD. EXT. is pressed. Key 10 is lit during external modulation.

2.3.3.3.3 Double Modulation

Simultaneous internal and external modulation is possible with the following combinations:

Internal	External
FM	AM
ΦM	AM
AM	FM or ΦM.

Set the modulation frequency as well as modulation depth, frequency or phase deviation or the internal modulation generator in accordance with section 2.3.3.3.1 while setting the same values for the external modulation on the modulation voltage source. The relationship between the voltage of the modulation generator and the modulation quantities is as follows:

FM 1 V_{rms} = 100 kHz

ΦM 1 V_{rms} = 5 rad

AM With double modulation the external modulation input is DC coupled for external amplitude modulation. Thus it can be used for external level control or as ALC input. The input voltage required is between 0 and +2.83 V, 0 V corresponding to the full carrier level and 2.83 V to a carrier reduction of about 40 dB.

For AM with sinewave modulation voltages and simultaneous superposition of a DC voltage of +1.41 V the relationship between modulation voltage and modulation depth is as follows:

1 V_{rms} = 100%. The internal modulation setting is displayed on 9 MODULATION.

2.3.3.3.4 Doubletone Modulation

The SMFP2 has two internal AF signal sources for the internal modulation:

1. a synthesizer for the frequency range 10 Hz to 25 kHz; for frequency setting see 2.3.3.4.
2. an AF generator 2 with the frequencies 400 Hz and 1 kHz.
   400 Hz is set with 200 REF,
   1 kHz is set with 201 REF.

Both signal sources are used for doubletone modulation. The modulation values can be separately adjusted for the two signals. The first signal is set through the normal modulation entry, the second is set with xxxx REF according to the relation xxxx = 2000 + modulation value (1000 max.)

FM 1000 = 10.00 kHz
ΦM 1000 = 1.000 rad
AM 1000 = 100.0 %

The AF synthesizer is chosen as the 1st signal source with 202 REF.

The AF generator 2 is chosen as the 1st signal source with 203 REF.

Example:

1st frequency 1.25 kHz from AF synthesizer with 4 kHz deviation
2nd frequency 400 Hz from AF generator 2 with 2 kHz deviation.

	FM	50
1.25	MOD. GEN	38
200	REF	29
202	REF	29
4	MOD. INT	8
2200	REF	29

2.3.3.4 Setting and Varying the AF (Audio frequency, modulation frequency)

Setting the AF frequency

To set the AF frequency, enter the desired numerical value in kHz via keyboard 25 (Fig. 2-3). Then press key 38 MOD. GEN. which defines the entered numerical value as an AF frequency. You need not enter either leading zeros before the decimal point, or trailing zeros after the decimal point; e.g. .01 kHz.

Moreover, with keys 12 FIXED FREQ. , one of the seven fixed frequencies

0.3, 0.4, 1, 1.25, 2.7, 3 and 6 kHz

can be selected.

If key 12 on the left-hand side is pressed 0.3 kHz is selected first, by pressing the next key 0.4 kHz is selected, etc. If key 12 on the right-hand side is pressed, 6 kHz is selected first.

The frequency selected according to the one or the other method is available at socket 34 MOD. GEN. It is displayed on 13 FREQUENZ NF/AUDIO. For setting the AF level, see section 2.3.3.5.

Varying the AF frequency

The frequency entered via key 25 can be varied in decade steps. To do so, set the cursor to the digit to be varied by means of the keys ⟸ ⟹.
By pressing one of the keys 22 "+" or "-" momentarily, the digit marked by the cursor is increased or decreased by one unit of the selected decade.
If the key is held down the AF frequency is varied continuously, first slowly, then after three steps at a faster rate. If the variation reaches the limit of the frequency range, LED 23 OVERFLOW lights up, indicating that the last command cannot be executed. The LED goes out if a new value which is within the frequency range is entered or key 25 "C" is pressed.

2.3.3.4.1 Selective Call Encoder

The AF Synthesizer also delivers selective calling signals according to CCIR or ZVEI. It is switched over to operate as a selective call encoder after entering 7 via the keyboard 25 and pressing the REF. key 29.

Then a 1-to 8-digit tone sequence can be called up by entering the tone codes 0 to 9 via the keyboard 25 and pressing the MOD. GEN. key 38. The entered tone sequence is repeated if either the MOD. GEN. key 38 or RECEIVER key 51 or TRANSMITTER key 49 is pressed.

When two successive tones are identical the repeat tone is used for the second tone.

ZVEI or CCIR tone code is selected by entering 8 or 9, respectively via the keyboard 25 and pressing the REF. key 29. At switch-on of the SMFP2 the ZVEI code is selected.

The selective call encoder is switched off by entering 6 via the keyboard 25 and pressing the REF. key 29.

NOTE: If the continuous tone present during normal operation is not desired prior and after the tone sequence, enter 0 via the keyboard 25 and press the MOD, GEN. key 38.

2.3.3.5 Setting and Varying the AF Level

Setting the AF level

The AF level at output socket 34 MOD. GEN. (Fig. 2-3) is selected by entering the desired numerical value in mV via keyboard 25. The numerical value entered is defined as the AF level by pressing the key 14 MOD. GEN.. The level is immediately set and displayed on 16 LEVEL. Key 14 lights up. Trailing zeros after the decimal point need not be filled in.

Varying the AF level

The AF level entered via keyboard 25 can be varied in decade steps. To do so, set the cursor to the digit on display 16 which is to be varied, by means of keys 22 ⟸ ⟹. By pressing keys 22 "+" or "-" momentarily the level increases or decreases by one unit of the selected decade. If the key is held down, the AF level is varied continuously, first slowly, then after three steps more rapidly.

If key 32 +20 dB is pressed the AF level is increased by 20 dB. The new value is then displayed on 16 and key 32 lights. If the key is pressed again the level is reduced by 20 dB to its previous value and the LED in the key goes out.

By pressing key 14 (MOD. GEN.) the increased level is transferred and the indicator in key 32 +20 dB goes off.

If the variation exceeds the limit of the range of adjustment LED 23 OVERFLOW lights.

2.3.3.6 Measurement of Level of External AF Signals

If key 15 EXT. NF/AC (Fig. 2-3) is pressed the AF level meter is switched on which permits the level of the signal externally applied to the socket NF-AC METER to be measured and displayed on 16 in mV. If key 17 CCITT is pressed a CCITT filter (300 Hz to 3 kHz) is switched into circuit and the level measured over a frequency range of 30 Hz to 20 kHz with CCITT weighting.

By entering 122 via the keyboard 25 and pressing the REF. key 29 a rejection filter can be cut into circuit during modulation or AF level measurement if no other measurement is switched on. The rejection filter (1 kHz, 300 Hz or 500 Hz) is selected by pressing the ⇕f key 18. The selected frequency is displayed on 13.

The rejection filter can be switched off by entering 123 via the keyboard 25 and pressing the REF. key 29.

2.3.3.7 SINAD Ratio Measurement

For measuring the SINAD ratio, to determine the receiver sensitivity, two measuring procedures are provided in the SMFP2. SINAD ratio measurement is only possible at 1 kHz. With the simple measuring procedure the SINAD ratio of the signal applied to socket 31 NF · AC METER is measured at the RF level and modulation given. This measuring procedure is called up by pressing key 19 SINAD if no numerical values have been entered. The measured value is displayed on 20. The circular quasi-analog display is assigned to the units digit.

With the automatic measuring procedure the SINAD ratio is measured and the RF Level varied - but not above -27 dBm - until the SINAD ratio entered via keyboard 25 and by pressing key 19 SINAD is reached. The SINAD ratio is displayed as with the simple measuring procedure. The RF level is displayed on 5.

With the automatic measuring procedure the measuring limit is ±2 dB. The average noise level is determined from 15 measurements.

By entering 4 via the keyboard 25 and pressing the REF. key 29 the measuring limit is switched over to ±1 dB. The average noise level is then determined from 50 measurements.

Reset to measuring limit ±2 dB by entering 3 via the keyboard 25 and pressing the REF. key 29.

2.3.3.8 S/N Ratio Measurement

The S/N ratio can be measured in the transmitter measurement mode or in the receiver measurement mode by pressing key 49 or key 51 respectively. The S/N ratio measurement is initiated by pressing key 21 and discontinued by pressing key 21 again.

Measurement of S/N ratio of transmitter section:
If no numerical values have been entered via keyboard 25, the S/N ratio of the demodulated transmitter signal is measured and displayed on 20.

Measurement of S/N ratio of receiver section:
If no numerical values have been entered via keyboard 25, the S/N ratio of the signal at socket 31 NF · AC METER is measured at the given modulation and displayed on 20.

If a numerical value has been entered in dB the RF level is automatically adjusted so as to obtain the selected S/N ratio - but not above -27 dBm to prevent the receiver from being damaged.

The RF level is read out on display 5 and the S/N itself on display 20. In the S/N measurement mode simultaneous quasi-analog display of the units digit is provided on 20.

With the automatic measuring procedure the measuring limit is ±2 dB. The average noise level is determined from 15 measurements.

By entering 4 via the keyboard 25 and pressing the REF. key 29 the measuring limit is switched over to ±1 dB. The average noise level is then determined from 50 measurements.

Reset to measuring limit ±2 dB by entering 3 via the keyboard 25 and pressing the REF. key 29.

During the automatic S/N ratio measurement the computer can be inhibited by pressing the RF OFF key 7. When this key is pressed again and the cable disconnected from the NF · AC METER socket 31, the inhibition is cancelled.

2.3.4 Transmitter Measurement

The transmitter measurement mode is selected by pressing key 49 TR. (Fig. 2-3) or by applying an RF signal > 0.5 W to socket 48 RF. In this operating mode, the SMFP2 measures the frequency, the power and the modulation of the signal applied to socket 48 RF. The values are displayed on 1, 5 and 9.
The AF generator supplies a frequency of 1 kHz.

2.3.4.1 RF Frequency Measurement

In the transmitter measurement mode, the frequency of the signal applied to socket 48 RF is measured. The result is displayed on 1.

If key 46 FREQ. MET. is pressed, the built-in frequency counter can be connected to the more sensitive input 47 FREQ. METER. The test result is also displayed on 1 in this case. The same is possible in the receiver measurement mode.

By entering 1 via keyboard 25 and pressing TRANSMITTER key 49 or FREQ. MET. key 46, the resolution of the frequency counter can be switched over from 10 Hz to 1 Hz. Reset to 10 by entering 10 via the keyboard 25 and pressing the key 49 or 46, respectively.

2.3.4.2 RF Level Measurement

In the transmitter measurement mode or by pressing key 45, the power at the RF socket 48 is measured. The result is displayed on 5 in W or dBm. By pressing key 45 again, the display is changed over from W to dBm, or vice versa.

In order to achieve the measurement accuracy guaranteed in the data sheet, it may be necessary to fit the coaxial 50-Ω resistor, which is supplied with the instrument, to rear socket 54.

An attenuator from 0 to 30 dB connected to the RF socket 48 can be taken into account when measuring power. To do so, the attenuation value must be entered. This is accomplished by entering 5 via the keyboard 25 and pressing the REF. key 29. Then enter the attenuation value, e.g. 6.3 via the keyboard 25 and press the W/dBm key 45. The entered attenuation value is also taken into account in the RF level setting. Thus the maximum output level is reduced by this value.

The RF level measurement cannot be performed when the measuring diode of the power meter is switched off. To avoid RF distortion of the attenuated signal at socket 54, the measuring diode of the power meter must be switched off.
To do so, enter 120 via the keyboard 25 and press the REF. key 29. The measuring diode can be switched on again by entering 121 via the keyboard 25 and pressing the REF. key 29.

2.3.4.3 Modulation Measurement

In the transmitter measurement mode the modulation depth, frequency or phase deviation of the signal applied to socket 48 (Fig. 2-3) is measured depending on the modulation type selected by means of keys FM, φM or AM. Keys 11 are disabled.

Keys 40 "-", $\frac{PK + PK}{2}$, "+" permit indication of the negative or the positive peak value or of the arithmetic mean to be selected. The selected value is displayed on 9.

Frequency deviations of < 100 Hz are considered spurious deviations and are indicated accordingly (rms weighting).

When measuring frequency and phase modulation audio frequencies over the range 5 Hz to 8 kHz are weighted. By pressing key 17 CCITT a filter is switched into circuit which permits the measurements to be weighted in accordance with CCITT (300 Hz to 3 kHz).
The AM measurement cannot be performed when the measuring diode of the power meter is switched off (see 2.3.4.2).

For rejection filter see 2.3.3.6.

2.3.4.4 AF Frequency Measurement

In the receiver measurement mode as well as in the transmitter measurement mode the frequency of a signal applied to socket 31 NF . AC METER (Fig. 2-3) can be measured. To do so, press key 33 EXT. NF/AC. The result is displayed on 13.

If key 36 DEMOD. FREQ. is pressed the frequency of the modulation signal is measured in the transmitter measurement mode (key 49 pressed) and displayed on 13.

If key 35 BEAT FREQ. is pressed the beat frequency between the signal applied to socket 47 FREQ. METER and the RF frequency from the signal entered via the keyboard is measured in the transmitter measurement mode. The result is displayed on 13.

The resolution of the RF counter can be switched over from 1 Hz to 0.1 Hz by entering 1 via the keyboard 25 and pressing the EXT. NF/AC key 33 or DEMOD. FREQ. key 36 or BEAT FREQ. key 35.

To reset it, enter 1 via the keyboard 25 and press 33 or 36 or 35.

2.3.4.5 DC Measurement

If key 30 U/I DC (Fig. 2-3) is pressed, the DC voltage applied to sockets 28 is measured and displayed on 16.

If key 30 is pressed again, the SMFP measures the direct current which flows via a resistance between the terminals + and -20 A (precision resistor 10 mΩ) or + and -200 mA (precision resistor 10 Ω). The result is displayed on 16. The Tester automatically switches over from the measurement range 20 A to 200 mA, and vice versa.

Watch for correct polarity when carrying out these measurements (see front panel). No indication is obtained if the polarity is not correct. Off-earth voltage and current sources may make it necessary to establish a reference earth.

2.3.4.6 Measurement on Transceivers with Acknowledgement Signal

- Initial settings

  Set the transmitter frequency to be measured, in the receiver measurement mode, and store with STO Ø. Then set the receiver frequency and the appropriate FM modulation (see section 2.1, function of the REF key 29).

- Measurement

  Switching selective call coder on with 7 REF:
  To call up acknowledgement signal measurement, enter the number 105 via the keyboard 25 and press the REF key 29.
  Send tone sequence with [CODE] NF GEN:
  After the transmitter has been keyed off, the Mobile Tester switches automatically to FM modulation measurement. The deviation meter is ready to measure within 70 ms (about 65 ms).
  The tone sequence received is indicated in display 1.

- Repeat measurement

  Select receiver measurement mode with EMPF 51.

  Send tone sequence with NF GEN.

- Switching off

  To cancel the measurement, enter the numerical value 106 via the keyboard 25 and press the REF. key 29.

2.3.4.7 High-speed Deviation Meter

The deviation meter can be preset which allows high-speed measurements, i.e. immediately at switch-on of the transmitter the demodulated signal is available at the demodulation output for further evaluation.

- Select transmitter measurement mode.
- Enter transmitter frequency minus 200 kHz (internal IF) via keyboard 25 and press SIGN. GEN. key.

  Example: Transmitter frequency .... 100 MHz
  Enter via keyboard .... 99.8 MHz
  and press SIGN. GEN. key.

2.3.4.8 Adjacent-channel Power Measurement (Only in conjunction with Option SMFPB 61)

Press key 49 to select transmitter test. Enter channel spacing (10 kHz, 12.5 kHz, 20 or 25 kHz) of the transceiver to be tested via keyboard 25 and store with one of the keys 2. The wanted-channel frequency in MHz of the transceiver under test can be entered via the keyboard 25 and stored by means of the SIGN. GEN. key 3.

The REF. 117 key 29 allows any channel spacing to be entered. Prior to such entry, measure the adjacent-channel power to select the appropriate measuring filters (bandwidth 4 kHz or 8 kHz at channel spacing 10/12.5 or 20/25 kHz, respectively. Reset to adjacent-channel power measurement with REF. 118 key.

The power in the upper adjacent channel can be called up by means of the "μW" key 43 and in the lower adjacent channel by means of pressing the "-" key on the keyboard 25 and then the "μW" key 43. The measured value is read out on the display 5. For display of the ratio of the adjacent-channel power to the wanted-signal power, press the "NKL dB" key 43 in place of the "μW" key.

2.3.4.9 Selective Call Decoding

All signals available at DEMOD. SIGN. output 37 are applied to the selective call decoder. If key 15 is pressed, the AF signal applied to socket 31 is also available at this output.

The decoder decodes and stores the frequencies listed in the following table; each tone of the CCIR or ZVEI tone sequence is evaluated as a code number if it is longer than 20 ms (also applies to continuous tone). The last seven codes are either displayed directly or interpreted accordingly if it is a repeat tone.

The tone code is selected according to section 2.3.3.4.2.

The memory content can be read out on display 1 any time by entering 11 via the keyboard 25 and pressing the REF. key 29.

After the content of the memory has been read out, the memory is cleared automatically to get ready for a new read-in process.

The memory of the selective call decoder can also be cleared manually by entering 10 via the keyboard 25 and pressing the REF. key 29.

Table

No.	CCIR(Hz)	ZVEI (Hz)	Readout	Explanation
0	1981	2400	0	Code number
1	1124	1060	1	
2	1197	1160	2	
3	1275	1270	3	
4	1358	1400	4	
5	1446	1530	5	
6	1540	1670	6	
7	1640	1830	7	
8	1747	2000	8	
9	1860	2200	9	
A	2400	2800	L	Group call
B	930	810	H	Data prefix
C	2247	970	P	
D	991	886	A	
E	2110	2600	like the preceding tone ("-" if it is the first tone of the sequence)	Repeat tone (invalid if it is the first tone of the sequence)
F	No tone	No tone	(blank)	Pause > 25 ms or no tone of standard sequence

2.3.4.10 Squelch Sensitivity

Call with 129 REF.

Function:

Reduce RF level until squelch function starts.

Increase RF level until squelch function stops.

Display on RESULT 20: squelch hysteresis in dB.

Display on LEVEL 5: RF level at which squelch function stops.

2.3.5 IEC Bus

The Mobile Tester SMFP2 can also be remote controlled. The data on the settings is transferred on a byte-serial bus using an interface that complies with the IEC 625-1 (formerly IEC 66.22) and IEEE 488-1975 standards as well as the DIN standard IEC 66.22. Connection is made at the rear of the Tester via the IEC 625 Bus socket 53 (Fig. 2-4). Fig. 2-5 shows the pin allocation.

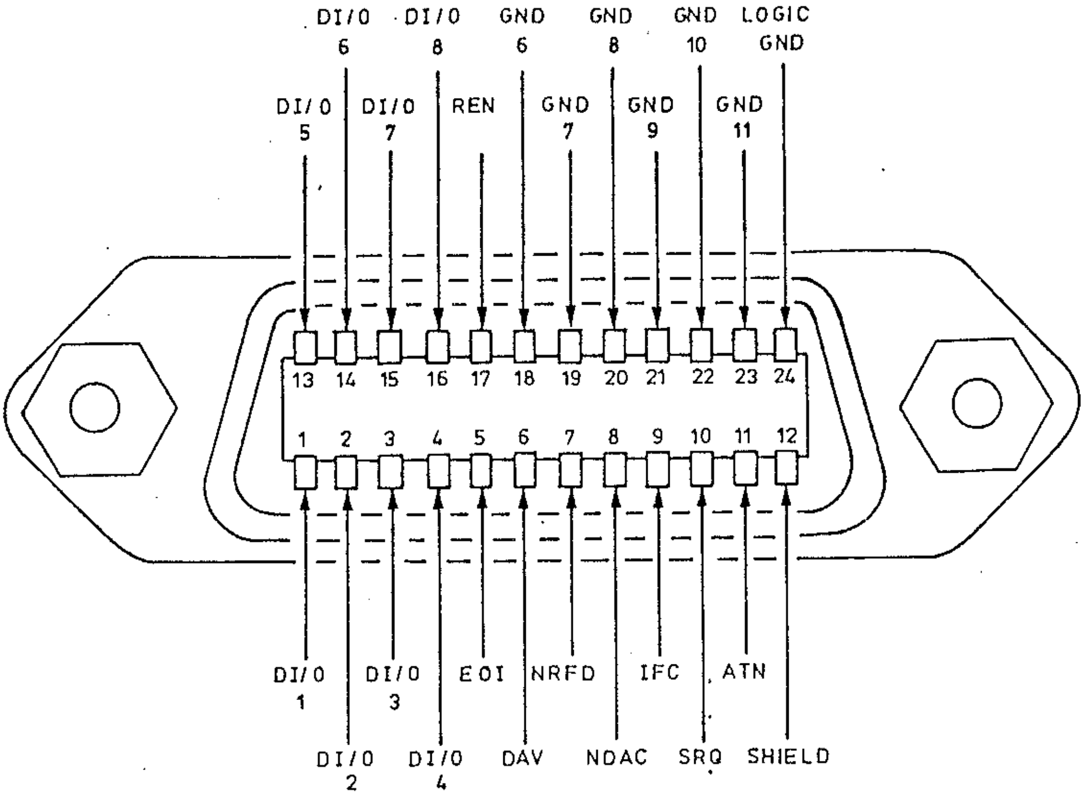


Fig. 2-5 Pin allocation

The interface connector specified by the American standard 488-1975 differs from that required by the international IEC standard. The SMFP2 is fitted with the 24-way interface connector, in accordance with the American standard 488-1975 which is more commonly used. Interconnection with instruments fitted with a 25-way interface connector in accordance with the IEC standard is readily possible by means of an adapter. Control functions and data transfer are identical in both cases.

The standard interface features three groups of bus lines:

1. Data bus - 8 lines DI/O to DI/O 8.
   Data transfer is bit-parallel and byte-serial, the characters being transferred in the ISO 7-bit or ASCII code. DI/O is the least significant bit and DI/O 8 the most significant.

2. Control bus - 5 lines.

This is used for the transfer of control functions:

ATN (Attention)	is active at low level during the transfer of an address to the connected device.
REN (Remote Enable)	is used for switching the device over to the remote control mode.
SRQ (Service Request)	By activating this line, a connected device can request the intervention of the controller.
IFC (Interface Clear)	is activated to bring the connected device into a defined initial condition.
EOI (End or Identify)	This signal can be used to mark the end of data transfer and is also used for polling after a service request. EOI signals are not processed in the SMFP2.

3. Handshake bus - 3 lines.

This is used for controlling the data transfer sequence:

NRFD (Not Ready for Data)	An active-low NRFD line indicates to the controller that one of the connected devices is not ready for data transfer.
DAV (Data Valid)	is activated by the controller shortly after a new data byte has been applied to the data bus.
NDAC (Not Data Accepted)	is kept active-low by the connected device until it has accepted the data present on the data bus.

In the IEC-bus system, the Mobile Tester functions as a listener or talker, i.e. it is capable of accepting data and executing setting commands from the controller and outputting the results of measurements.

2.3.5.1 Setting the Address

Before the Tester is connected to the IEC bus, set a suitable device address on the Tester by means of address switches A1 to A5. The address switch A6 must always be in the OFF position.

The coding switch ADDRESS 55 (Fig. 2-6) is located on the rear panel (Fig. 2-4).

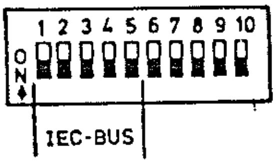


Fig. 2-6 Coding switch.

The following table shows the settings required for the various possible addresses. The SMFP2 is supplied from the factory with device address setting 30.

Table 2-1

ASCII character		Binary address					Decimal equivalent
Listen address	Talk address	Address switch A5	A4	A3	A2	A1	
(SPACE)	@	0	0	0	0	0	0
!	A	0	0	0	0	1	1
"	B	0	0	0	1	0	2
#	C	0	0	0	1	1	3
$	D	0	0	1	0	0	4
%	E	0	0	1	0	1	5
&	F	0	0	1	1	0	6
'	G	0	0	1	1	1	7
(	H	0	1	0	0	0	8
)	I	0	1	0	0	1	9
*	J	0	1	0	1	0	10
+	K	0	1	0	1	1	11
,comma	L	0	1	1	0	0	12
-	M	0	1	1	0	1	13
.	N	0	1	1	1	0	14
/	O	0	1	1	1	1	15
0	P	1	0	0	0	0	16
1	Q	1	0	0	0	1	17
2	R	1	0	0	1	0	18
3	S	1	0	0	1	1	19
4	T	1	0	1	0	0	20
5	U	1	0	1	0	1	21
6	V	1	0	1	1	0	22
7	W	1	0	1	1	1	23
8	X	1	1	0	0	0	24
9	Y	1	1	0	0	1	25
:	Z	1	1	0	1	0	26
;		1	1	0	1	1	27
<		1	1	1	0	0	28
=		1	1	1	0	1	29
>		1	1	1	1	0	30

When entering data, the setting range limits must be observed. When the range limits are exceeded, the LED OVERFLOW 23 lights. If the resolution of the entries is higher than the setting resolution of the Tester, the entries will be rounded to the nearest possible value.

2.3.5.2 Data Format

In accordance with the IEC draft standard the SMFP2 requires the following format for data transfer (Table 2-2):

Each instruction to change a setting consists of at least an initial character (header) and a final character (delimiter). When data on a setting is to be transferred, enter the data between these two limiting characters. All characters are transmitted in ISO 7-bit (ASCII) code.

After a measurement has been completed, the result of the measurement must be called up before a new measurement is made, since otherwise the data of the second measurement would be written over the data of the first measurement.

The delimiter for the output is defined in the Tester as CR. If a faulty string is entered, a Service Request (SRQ) is sent via the IEC bus.

With the Mobile Tester, three decade BCD outputs and nine relays can be activated via the IEC bus. These outputs are brought out at the two 15-way sockets BU401 and BU402 (57, 59) Fig. 2-4.

The control contacts and control instructions are listed in Tables 2-2 to 2-4.

Manually-controlled functions that are not mentioned here cannot be remote controlled.

Table 2-2 SMFP2 keyboard control via IEC bus

CONTROL FUNCTIONS:		CODE	
REC.		AR	
XMTR		(AT)	
AM	(INT)	AA	
FM	(INT)	AB	
PHIM	(INT)	AC	
FM	(EXT)	BI	
PHIM	(EXT)	BJ	
AM	(EXT)	BK	
RF OFF	(ON)	D@	
RF OFF	(OFF)	E@	
CCITT	(ON)	EC	
CCITT	(OFF)	DC	
STORE	90	DSØ	
	.	.	
	.	.	
	.	.	
STORE	95	DS5	
RECALL	90	DRØ	
	.	.	
	.	.	
	.	.	
RECALL	95	DR5	
FUNCTIONS OF REF KEY		BO (value)	(value = numerical value of function)
INPUT FUNCTIONS:			
SIGN GEN		AG	VALUE IN MHZ
MYV	<with fine adj.>	AI <XI>	VALUE IN MYV
MIV	<with fine adj.>	AJ <XJ>	VALUE IN MIV
DBM	<with fine adj.>	AK <XK>	VALUE IN DBM
DMBYV	<with fine adj.>	AL <XL>	VALUE IN DBMYV
-Ø.1DB RF LEVEL		DK	
+Ø.1DB RF LEVEL		EK	
MOD INT (ON)		AM	VALUE IN %,KHZ OR RAD
MOD INT (OFF)		EM	
MOD EXT (ON)		AZ	VALUE IN %,KHZ OR RAD
MOD EXT (OFF)		EZ	
MOD GEN (FREQ)		AO	VALUE IN KHZ
MOD GEN (LEVEL)		AQ	VALUE IN MIV
-DELTA F		AD	VALUE IN KHZ
+DELTA F		AE	VALUE IN KHZ
STORE Ø		B@,ZZØ	
1		B@,ZZ1	
2		B@,ZZ2	
3		B@ (VALUE),ZZ3	VALUE IN KHZ
4		B@ (VALUE),ZZ4	VALUE IN KHZ
5		B@ (VALUE),ZZ5	VALUE IN KHZ
RECALL Ø		A←,ZZØ	
1		A←,ZZ1	
2		A←,ZZ2	
3		A←,ZZ3	BZW A←,ZZ-3
4		A←,ZZ4	BZW A←,ZZ-4
5		A←,ZZ5	BZW A←,ZZ-5

ASCII CHARACTERS:

DEZ.	HEX.
@64	40H
←95	5FH

TEST FUNCTIONS:		OUTPUT:	
FREQ MET	AF	AF........E-.	MHZ
RF FREQ	AT	AF........E-.	MHZ
POWER IN W	AW	AW....E-.	WATT
POWER IN DBM	BL	BL....E-.	DBM
NKL DB (LOWER CHANNEL)	AN+ OR AN-	AN....E-.	DB
NKL MYW (LOWER CHANNEL)	BZ+ OR BZ-	BZ....E-.	MYW
+	BF	BF....E-.	%, KHZ, RAD
PK+PK/2	BG	BG....E-.	%, KHZ, RAD
-	BH	BH....E-.	%, KHZ, RAD
EXT AF(FREQ)	AP	AP........E-.	KHZ
DEMOD FREQ	AU	AU........E-.	KHZ
BEAT FREQ	AV	AV........E-.	KHZ
EXT.AF(LEVEL)	AX	AX....E-.	VOLT
V/I	EY	EY....E-.	VOLT
CURRENT	DY	DY....E-.	AMPERE
DISTORTION 1KHZ	EE	EE... E-.	%
3ØØHZ	ED	ED...E-.	%
5ØØHZ	EG	EG...E-.	%
SINAD	AS	AS...E-.	DB
SINAD (AUT.)	AS(VALUE)	AS...E-.DBM	
REC. S/N	BB	BB...E-.	DB
REC. S/N (AUT.)	BB(VALUE)	BB...E-.DBM	
XMTR. S/N	BB	XB... E-.	DB
PROBE IN V	FL1	FL....E-.V	VOLT
PROBE IN DBM	FLØ	FL....E-.D	DBM
BANDWIDTH MEASUREMENT	BO115	EH........E-.	MHZ
BANDWIDTH MEASUREMENT	BO116	EI........E-.	MHZ
QUIETING	BO119	QU....E-.	DB
SQUELCH SENSITIVITY	BO129	SQ....E-.DBM,..E-.	DB
AUT.NOM.DEVIATION ADJUSTMENT	BO2	AQ....E-.	MV
SELECTIVE CALL DECODER	BO11	TD........	FOR EXPLANATION OF THE CHARACTERS SEE TABLE 2-4

SRQ CALLS:

STATUS (READ IN BY SERIAL POLL)

68 ERROR IN IEC INSTRUCTION (INPUT ERROR)
70 OVERFLOW
71 MEASUREMENT TERMINATED
72 MEASUREMENT TERMINATED WITH OVERFLOW

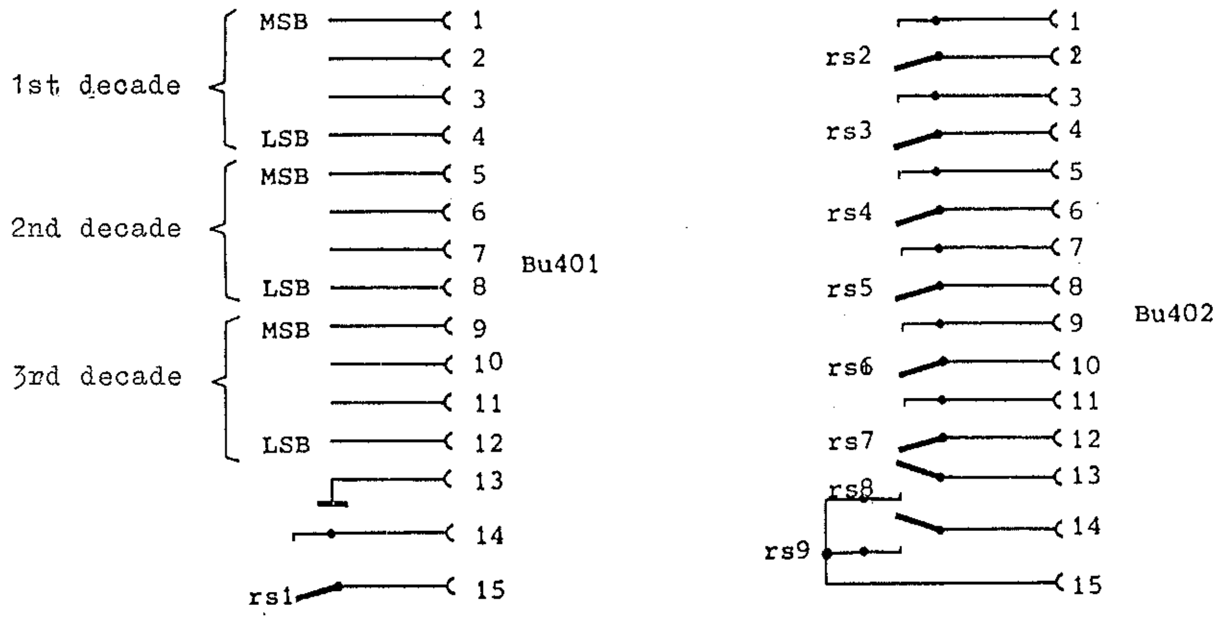
EXAMPLE IN BASIC WITH PPC:

READOUT OF TEST RESULT AFTER SRQ CALL:

```
1ØØ IECTERM13:IECTIMES
12Ø IECSRQ THEN GOTO 1ØØØ
13Ø B$="AX":REM AF LEVEL MEASUREMENT
14Ø IECOUT30,B$
15Ø X=Ø
16Ø IECTERM13:IFX=Ø THEN GOTO16Ø
17Ø END
1ØØØ IECSPL3Ø,V%
1Ø1Ø IFV%=68 THEN PRINT "INPUT ERROR"
1Ø2Ø IFV%=70 THEN PRINT "OVERFLOW"
1Ø3Ø IFV%=71 THEN GOSUB2ØØØ
1Ø4Ø IFV%=72:PRINT "OVERFLOW":GOSUB2ØØØ
1Ø5Ø IECRETSRQ
2ØØØ IECIN3Ø,Y$:PRINT Y$
2Ø1Ø X=1
2Ø3Ø RETURN
```

Table 2-3 IEC OUTPUTS BU401, BU402

Pin allocation:



Relay I is switched on by means of key 49 TR and switched off by means of key 51 REC.

Table 2-4 IEC instruction code

Decades:	EA XYZ
X : numerical value	1st decade
Y : numerical value	2nd decade
Z : numerical value	3rd decade

HEX	Dec	X,Y or Z as ASCII character
0	0	0
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
A		:
B		;
C		<
D		=
E		>
F		?

Relays:	EF XY
X : relay number	
Y = 0 : open relay	
Y = 1 : close relay	

Table 2-5

Examples of IEC-bus instructions

Instructions	Tektronix 4051,4052	hp 9825	hp 9835/9845	Commodore PET 2001/3001	R&S PPC
Presettings	---	---	---	Open 1,30	---
Frequency 123.5 MHz	PRINT@ 30:"AG123.5 "	wrt730,"AG123.5 "	OUTPUT730;"AG123.5 "	PRINT# 1,"AG123.5 "	IECOUT30,"AG123.5 "
Frequency as a variable	LET F=123.5 PRINT@ 30:"AG";F;	F=123.5 wrt730,"AG",F	LET F=123.5 OUTPUT730;"AG";F;	LET F=123.5 PRINT# 1,"AG";STR$(F);	F=123.5 **) IECOUT30,"AG"+STR$(F)+
Level -24.8 dBm	PRINT@ 30:"AK-24.8 "	wrt730,"AK-24.8 "	OUTPUT730;"AK-24.8 "	PRINT# 1,"AK-24.8 "	IECOUT30,"AK-24.8 "
Fine variation -0.1 dBm +0.1 dBm	PRINT@ 30:"DK " PRINT@ 30:"EK "	wrt730,"DK " wrt730,"EK "	OUTPUT730;"DK " OUTPUT730;"EK "	PRINT# 1,"DK " PRINT# 1,"EK "	IECOUT30,"DK " IECOUT30,"EK "
Modulation FM internal 2.8 kHz deviation	PRINT@ 30:"AB " PRINT@ 30:"AM2.8 "	wrt730,"AB " wrt730,"AM2.8 "	OUTPUT730;"AB " OUTPUT730;"AM2.8 "	PRINT# 1,"AB " PRINT# 1,"AM2.8 "	IECOUT30,"AB " IECOUT30"AM2.8 "
Measurements +) Frequency/MHz	PRINT@ 30:"AF " INPUT@ 30,F$	wrt730,"AF " red730, F$	OUTPUT730;"AF " ENTER730;F$	PRINT# 1,"AF " INPUT# 1,F$	IECOUT30,"AF " IECIN30,F$ *)
Level/W	PRINT@ 30:"AW " INPUT@ 30,F$	wrt730,"AW " red730,F$	OUTPUT730;"AW " ENTER730;F$	PRINT# 1,"AW " INPUT# 1,F$	IECOUT30,"AW " IECIN30,F$ *)
AM/% Pos. modulation depth	PRINT@ 30:"AA " PRINT@ 30:"BF " INPUT@ 30,F$	wrt730,"AA " wrt730,"BF " red730,F$	OUTPUT730;"AA " OUTPUT730;"BF " ENTER730,F$	PRINT# 1,"AA " PRINT# 1,"BF " INPUT# 1,F$	IECOUT30,"AA " IECOUT30,"BF " IECIN30,F$ *)

+) The test result of these examples is stored under the variable F$ (cf. Table SMFP keys IEC bus).

*) Preparation of PPC for reading in: IECTIME50 (waiting time)
IECTERM13 (<CR> as delimiter)

**) For string processing make sure that no unwanted characters are included. This is absolutely essential with the commands for relay control and the BCD outputs.

Example with PPC: IECOUT30, "EA" + MID$ (STR$(F), 2)+","

Table 2-6

	Tektronix 4051/4052	hp 9825	hp 9835/9845	Commodore PET 2001/3001	R&S PPC
Go to Local	WBYTE@ 62,1:	lcl730	LOCAL730 or LOCAL7	No capability	IECLAD30 IECGTL IECUNL
Local lockout	WBYTE@ 62,17: or WBYTE@ 17:	llo7 (for all devices)	LOCAL LOCKOUT7 (for all devices)	" "	IECLLO
Remote	WBYTE@ 62:	rem730 or rem7	REMOTE730 or REMOTE7	Only in connection with an output	IECREN and IECLAD30,"
Selected device clear	WBYTE@ 62,4:	clr730	RESET730	No capability	IECLAD30 IECSDC IECUNL

Table 2-6 lists examples of the output of particular instructions. The decimal address of the SMFP2 is assumed to be 30. This decimal address corresponds to the full decimal equivalent 62.

2.5 Retrofitting Options

Before fitting an option, pull out power plug. Never change circuit boards unless the SMFP2 is switched off.

2.5.1 Fitting the Reference Oscillator Option SMS-B1

Remove bottom of case and open bottom of cassette. Pull out reference circuit board Y6 (302.6215; yellow/red colour coding). Unplug the two links BR1 and BR2 on the circuit board. Insert the SMS-B1 and screw in place by means of the three screws supplied with it. Replace circuit board Y6 in the cassette and put cover of cassette back on. Replace bottom of case.

2.5.2 Fitting the 1-GHz Frequency Extension Option SMFP-B2

Space for accommodation of this option is reserved in the rear left-hand corner of the SMFP2.

Preparations:

- Remove bottom and top sections of the cabinet.
- Remove strip from the left side panel.
- Remove RF cable K2 between ST15 of the cassette and the attenuator.

Mounting the option:

Insert the option in the rear left-hand corner of the SMFP2 with the RF connectors pointing upwards and loosely fix to the side panel with four screws M 2.5 x 8. After fixing it to the rear panel with two screws M 2.5 x 8, tighten down the four screws on the side panel.

Routing of the cables supplied with the option: *

- Run the RF cable K2 between ST15 of the cassette and ST442 of the option.
- Run the RF cable K441 between ST441 of the option and the RF terminal (BU1) of the attenuator.
- Connect the flat cable K45 to ST45 of the Motherboard III (for location of ST45 and pin numbers, see Components Location Plan 332.3114, sheet 3).

* Note: Use a torque wrench for fitting the SMA sockets of the attenuator.
Torque range: 80 to 120 N/cm.

Retrofitting the option reduces the RF output level of the SMFP2 by about 0.8 dB.

It is therefore necessary to readjust the Modulation Control board Y10 (302.7011) accordingly.

a) Level correction:
   Settings on the SMFP2: UNMOD, 3 dBm
   Adjust the RF output power to 3 dBm by means of potentiometer R76 on Y10.
   Determine frequency response between 400 kHz and 520 MHz.

b) Modulation depth correction:
   Settings on the SMFP2: 130 MHz, 80% AM INT., 1 kHz, 3 dBm
   Adjust the modulation depth of the RF output signal to 80% by means of the potentiometer R79 on Y10.
   Determine the frequency response between 400 kHz and 520 MHz.

The IC supplied extends the count range of the RF counter.
To fit

- loosen subminax cable on board 332.2118
- remove board
- loosen shielding cover
- insert IC (B23 in circuit diagram or components location plan 332.2118)
- close cover. Then insert and connect the board.

Change the frequency range plate on the front panel to show the extended frequency range, i.e. 0.4 to 1000.

Replace bottom and top of case.

2.5.3 Fitting the Adjacent-channel Power Meter Option SMFPB61

- Remove cable K3 (2nd RF generator output - mixer).
- Insert board in the space provided for this purpose (black/green colour coding).
- Connect cables supplied with the option:
  RF generator - Adjacent-channel Power Meter board and Adjacent-channel Power Meter board - mixer.

2.5.4 Fitting the 60-W Option SMFP2B3

- Remove upper and lower cover panels.
- Remove carrying handle.
- Remove left trim strip (four screws).
- Remove left side wall (nine screws).
- Remove cable K1.

In the place of cable K1 fit the 60-W Option with the two cables supplied with it.

Reassemble the SMFP2. Screw the heat sink of the Option to the inside of the left side wall by means of the four screws supplied.

Connect the link BR12 on the computer board Y21 to ⊥ (identification signal changed over).

Close the unit again.

2.5.5 Fitting the RF Millivoltmeter Option SMFS2B8

Remove upper and lower cover panels.

Remove the plastic cover from the front panel and mount in its place the 3-way connector and cable supplied with the option.

Insert the RF Millivoltmeter Option board instead of the adapter board (colour code white-white, at the front, on the left-hand side).

Wire as follows:

- Connect cable from the front panel to connector 2.
- Connect the RF Millivoltmeter Option to connector 122 on the front motherboard. Prior to do so, remove the plugs from the motherboard.
- If the Analog Display Option SMFS-B9 is fitted, connect it to the RF Millivoltmeter via the 2-core cable of B9 (B8, ST4 - B9, ST91).

Close the unit again.

2.5.6 Fitting the Selective Call Decoder Option SMFS2B6

The SMFS2B6 is mounted on top of the digital section (colour code white-yellow).

Remove the upper cover panel.
Pull out the digital PC board towards the top.

Connect the option to the base plate via the 16-way connector ST243 and tighten down with three screws. Replace the PC board, connect it and close the SMFP2 again.

3. Maintenance

3.1 Mechanical Maintenance

Mechanical maintenance is restricted to cleaning the air-filter mesh screen.

If the air filter is not cleaned properly, the set may be damaged due to overheating.

The blower motor is a brushless type and does not require any maintenance.

3.2 Electrical Maintenance

3.2.1 Measuring Instruments Required

Table 3-1

Ref. No.	Instrument	Performance ratings	R&S type	See section
1	RF counter	Range 0.4 to 520 MHz Resolution 10 Hz		3.2.2.2 3.2.2.19
2	Power meter	Range 0.4 to 520 MHz 3 to 20 mW Z = 50 Ω Error < 0.1 dB	NRS 100.2433.92	3.2.2.3 3.2.2.4 3.2.2.15 3.2.2.19 3.2.2.20
3	Standard attenuator	Range 0.4 to 520 MHz 0 to 120 dB, Z = 50 Ω	DPVP 214.8017.52	3.2.2.5
4	Test receiver Frequency controller	Range 25 to 520 MHz Inherent noise < -10 dB/μV	ESU 2 252.0010.52 EZK 255.0010...	3.2.2.5
5	RF wave analyzer	Range 0.4 to 1100 MHz Dynamic range > 70 dB		3.2.2.6 3.2.2.7
6	AF generator	Range 50 Hz to 20 kHz Output voltage > 1 V Zout = 600 Ω Distortion < 0.2%	SPN 336.3019.02	3.2.2.8 3.2.2.9 3.2.2.10 3.2.2.11 3.2.2.12 3.2.2.13 3.2.2.18 3.2.2.21 3.2.2.22 3.2.2.26 3.2.2.28 3.2.2.29

Ref. No.	Instrument	Performance ratings	R&S type	See section
7	Test demodulator	RF range 0.4 to 520 MHz AF range 50 Hz to 20 kHz AM: 0 to 90% FM: 0 to 125 kHz deviation Distortion < 0.2%	FAM 334.2015.53	3.2.2.8 3.2.2.9 3.2.2.10 3.2.2.11 3.2.2.13 3.2.2.21 3.2.2.22 3.2.2.23
8	Distortion meter	Range 50 Hz to 20 kHz Measurement range 0.1 to 10%		3.2.2.10 3.2.2.12 3.2.2.18 3.2.2.28 3.2.2.29
9	AF counter	Range 0.1 to 25 kHz Resolution 1 Hz		3.2.2.18
10	DC power supply	V 0.01 to 30 V I 0 to 10 A	NGRS 100.5090.02	3.2.2.15 3.2.2.17 3.2.2.24 3.2.2.25
11	Deviation meter	Range 0.4 to 520 MHz Inherent spurious deviation < 1.5 Hz (CCITT)	FAM + FAM-B6 334.2015.53 334.5614.02	3.2.2.14
12	Phsophometer	Min. input voltage 0.1 V with CCITT weighting filter and rms value detector	UPGR 248.1915...	3.2.2.14 3.2.2.18 3.2.2.21 3.2.2.22
13	Precision transmission line	Z = 50 Ω	SWOB-Z 100.3598.50	3.2.2.16
14	RF millivoltmeter with insertion unit	Range 1 to 520 MHz Sensitivity 100 mV	URV 216.3612...	3.2.2.16
15	Controller	Interface to IEEE 488 and IEC 625.1		3.2.2.30
16	Power signal generator	Frequency range 25 to 1000 MHz Power ≧ 2 W Z = 50 Ω	SMLU 200.1009...	3.2.2.17 3.2.2.20 3.2.2.21 3.2.2.22
17	RF power amplifier			3.2.2.20
18	Digital multimeter		UDL 4 346.7800.02	3.2.2.24 3.2.2.25

3.2.2 Performance Check

3.2.2.1 Checking the Functioning of Display and Keyboard

Check switch-on state: After switching on, the following must be displayed:

Frequency	Level	Modulation	Frequency	Level	Result

IA30 refers to the IEC-bus address set on the rear.

If no transceiver (transmitter) is connected, the following readouts are obtained after three seconds:

Frequency	Level	Modulation	Frequency	Level	Result
000.0000	000	.000 kHz	1.000 kHz	1,0 mV ▲	000

and the following keys light:

FM (50)	FM (11)	Mod. Gen. (38)	Mod. Gen. (14)
TR.(49)	PK + (40)		

To check keyboard, make entries according to section 2.3 and observe display.

3.2.2.2 Checking the Frequency Setting and Accuracy

Settings: UNMOD., level approximately 100 mV.

Test setup: Connect frequency meter to RF output 48.

Test: Set following frequencies and check with frequency counter:

100	320.0024	445.75
150	340.0048	445.775
280	340.0049	445.8
281	340.0050	445.85
285	340.0052	445.95
293	340.0056	446.55
297.9901	340.0064	447.35
309	340.0080	448.95
318.0001	340.0112	452.165
318.0152	340.0176	458.6
	340.0304	445.725
	399.8727	

Permissible relative frequency error:

1×10^{-6}/month + 1×10^{-6}/ °C (standard reference oscillator)

5×10^{-8}/month + 1×10^{-7} in the range 0 to 50°C (reference oscillator option)

After warmup, the relative frequency error must be the same at all frequencies.

3.2.2.3 Checking the Error and Frequency Response of the Output Level

Settings: a) UNMOD., level 13 dBm
b) AM, m = 0, level 5.1 dBm.

Test setup: Connect power meter to RF output 48.

Test: Measure output level between 0.4 and 520 MHz.
Permissible frequency response (difference between maximum and minimum level) is
≦ 1.8 dB (0.4 to 8 MHz)
≦ 0.8 dB (8 to 520 MHz).

The permissible error of the output level (deviation from level set) is
≦ ±1.8 dB (0.4 to 8 MHz)
≦ ±1.3 dB (8 to 520 MHz).

3.2.2.4 Checking the Fine Level Adjustment

Settings: UNMOD., level 11.1 dBm, frequency 130 MHz.

Test setup: Connect power meter to RF output 48.

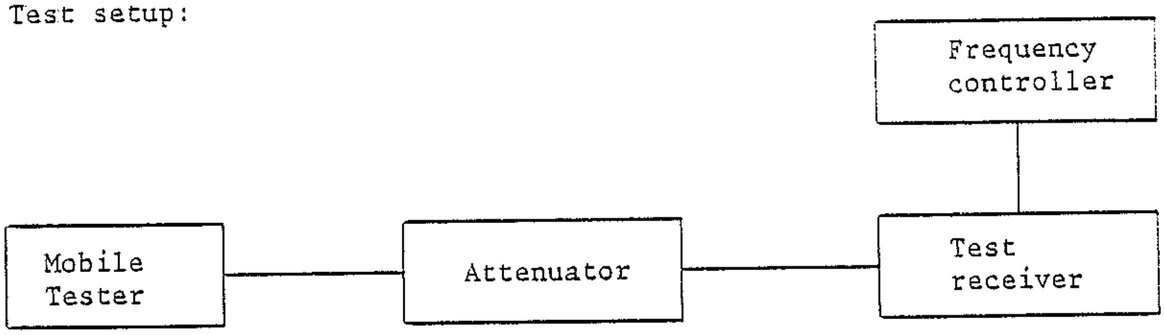
Test: Reduce level to 1.1 dBm by means of 0.1-dB key and check level steps on the power meter.
Permissible deviation is ±0.5 dB at 1.1 dBm.

If level has dropped below 1.1 dBm during fine adjustment, re-enter level of 11.1 dBm and subsequently reduce it by means of the 0.1-dB key.

3.2.2.5 Checking the RF Attenuator Error

Settings: UNMOD., level 13 dBm, frequency 131 MHz.

Test setup:



Test: Set attenuator to 112 dB.
Set test receiver to a frequency of 131 MHz and select 3-mV range and 15-kHz bandwidth. Then check level at following settings:

Table 3-2

Level Mobile Tester	Attenuation Attenuator
13 dBm	112 dB
11 dBm	110 dB
9 dBm	108 dB
5 dBm	104 dB
3 dBm	102 dB
- 7 dBm	92 dB
-27 dBm	72 dB
-67 dBm	32 dB
-87 dBm	12 dB

Permissible level error referred to 13 dBm level setting is $\leqq$ ±0.2 dB.
The control signals for the RF attenuator can be checked against Table 4-5.

3.2.2.6 Checking the Level of Non-harmonic Spurious Signals

Settings: UNMOD., level 3 dBm, frequency 0.4 to 520 MHz.

Test setup: Connect RF wave analyzer to RF output 48.

Test: Level of non-harmonic spurious signals in the range 0.4 to 520 MHz is to be checked at the following frequencies:

Table 3-3

Frequency setting on the Mobile Tester	Frequency of non-harmonic spurious signals
Range 0.4 to 129.9999 MHz	380 + $f_{Mobile\ Tester}$
	380
129	251
Range 110 to 129.9999 MHz	380 -2 $f_{Mobile\ Tester}$
Range 75 to 129.9999 MHz	380 -3 $f_{Mobile\ Tester}$
319	40, 340
320	80, 300
439	80, 460
440	40, 420

Minimum level of non-harmonic spurious waves: down ≧ 60 dB.

3.2.2.7 Checking the Level of Harmonics

Settings: UNMOD., level 3 dBm, frequency 0.4 to 520 MHz.

Test setup: Connect RF wave analyzer to RF output 48.

Test: Minimum level of harmonics in the range 0.4 to 520 MHz: down ≧ 30 dB.

3.2.2.8 Checking the Modulation Attenuator

Settings: FM EXT., deviation 100 kHz, level 3 dBm, frequency 460 MHz.

Test setup: See section 3.2.2.10.
Modulation signal 1 kHz. Vary voltage until deviation of 100 kHz is measured.

Test: Set following deviations and check with modulation meter:
9, 16, 16.5, 17, 18, 20, 24, 32, 64 kHz.

Permissible deviation: ±2%.

NOTE: Select narrow enough AF bandwidth (e.g. 3 kHz) on the demodulator to ensure that no additional error due to noise is obtained when measuring small deviations.

3.2.2.9 Checking the FM Error

Settings: FM, deviation 100 kHz, level 3 dBm,
150, 250, 460, 500, 920*), 1000*) MHz

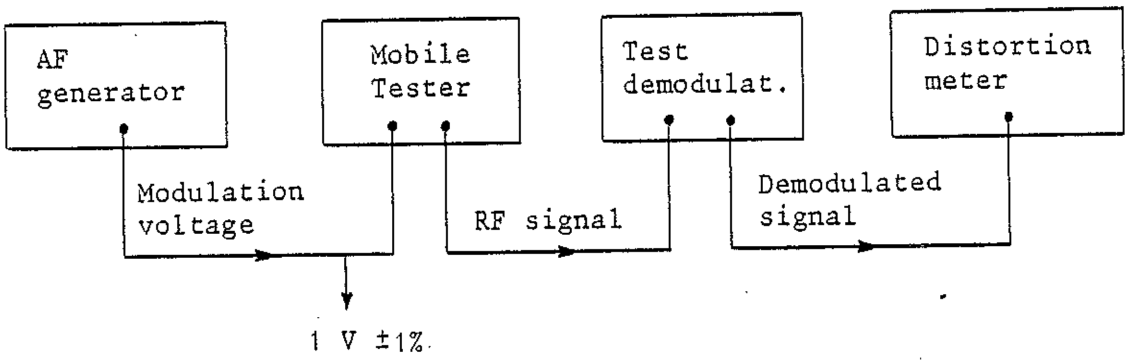
Test setup: See section 3.2.2.10.
Modulation voltage 1 V ±1%.

Test: Permissible error of frequency deviation at modulation frequencies of 0.4 to 20 kHz: ≦ ±5%.

3.2.2.10 Checking the FM Distortion

Settings: FM, level 3 dBm.

Test setup:



Test: Check modulation distortion at following settings:

Table 3-4

Frequency of the Mobile Tester (MHz)	Modulation frequency	Deviation	Permissible distortion
150; 520	400 Hz to 2 kHz	75 kHz	≦ 1%
90; 400; 500; 510; 520	20 kHz	20 to 75 kHz	≦ 5%

*) If fitted with Option SMFP B-2.

3.2.2.11 Checking the AM Error

Settings: AM 1 to 90%, level 5.1 dBm

a) 0.4 MHz, 5 MHz
b) 350 MHz

Test setup: See section 3.2.2.10.

Test: Check error of modulation depth at following frequencies:

Table 3-5

Frequency	Modulation frequency
a) 0.4/5 MHz	0.4/5 kHz
b) 350 MHz	0.4/20 kHz

Permissible error: a) < ±8%
b) < ±5%

3.2.2.12 Checking the Envelope Distortion

Settings: AM 80%, level 5.1 dBm

a) 0.4/5 MHz
b) 350 MHz

Test setup: See section 3.2.2.10.

Test: Measure envelope distortion at following frequencies:

Table 3-6

Frequency	Modulation frequency	Permissible distortion
a) 0.4/5 MHz	1 kHz	≦ 1.5%
	5 kHz	≦ 5%
b) 350 MHz	1 kHz	≦ 1.5%
	20 kHz	≦ 5%

3.2.2.13 Checking the Phase Modulation

Settings: MOD. EXT. φM

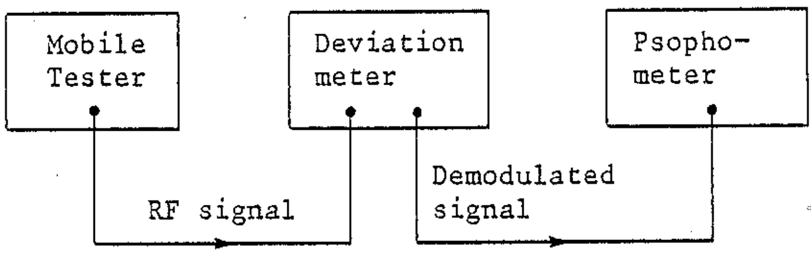
Test setup: See section 3.2.2.10.

Test: Apply AC voltage of 1.00 V ±1% to socket 39 MOD. EXT. This must produce a phase modulation of 5 rad (±5%). This corresponds to a deviation of 5 kHz at a modulation frequency of 1.00 kHz.

3.2.2.14 Checking the Spurious Deviation

Settings: UNMOD., level 3 dBm, frequencies 129 MHz, 520 MHz.

Test setup:

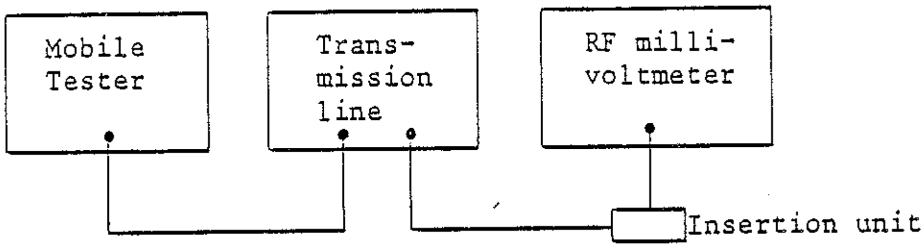


Test: Measure spurious deviation by means of CCITT weighting filter (0.3 to 3 kHz) and rms-value rectifier. (The inherent spurious deviation of the deviation meter used must be < 1.5 Hz.) Permissible spurious deviation: ≦ 4 Hz.

3.2.2.16 Checking the VSWR

Settings: AM 0%, level -3 dBm, frequency 100 to 520 MHz.

Test setup:



Test: Vary test frequency until a voltage maximum is measured. Subsequently vary frequency (Δf = 7.5 MHz with a cable length of 10 m) until adjacent voltage minimum is measured.

$$VSWR = \frac{V_{max}}{V_{min}}$$

3.2.2.17 Checking the Response Threshold of the Overload Protection

Settings: REC. 51, FM 50, level 0 dBm, frequency 130 MHz.

Test setup 1: Feed DC voltage (any polarity) to RF input/output 48. Increase from 0 V to 6 V.

Test: Between 2 V and 5 V, the overload protection must respond (audible). The LED of the REC. key 51 goes out and the LED of the TR. key 49 lights up.

Test setup 2: Apply RF power from power signal generator (25 to 1000 MHz) to same input. Increase from 0 W to 2 W.

Test: At P = 0.1 to 1 W, the overload protection must respond.

3.2.2.18 Checking the Modulation Generator (AF synthesizer)

3.2.2.18.1 Checking the Frequency Setting and Accuracy

Settings: Level mod. gen. approx. 1000 mV.

Test setup: Connect frequency meter to output 34 MOD. GEN. (after warm-up of SMFP2).

Set following frequencies on SMFP2 and check by means of frequency counter:

19 Hz	1211 Hz	9440 Hz	9300 Hz
38.1 Hz	2403 Hz	9412 Hz	9272 Hz
76.1 Hz	9469 Hz	9384 Hz	9245 Hz
152.2 Hz	18380 Hz	9356 Hz	9218 Hz
607.9 Hz		9328 Hz	

The relative frequency error $< 1 \times 10^{-6}$ for f < 15 kHz and $< 1 \times 10^{-5}$ for > 15 kHz must be added to the relative frequency error of the reference frequency.

Checking the fixed frequencies: Settings and test setup as above. Call up all seven fixed frequencies once by means of respective keys and check using frequency counter.

3.2.2.18.2 Checking the Distortion

Settings: Level mod. gen.: 5000 mV and 100 mV,
frequency mod. gen: 50 Hz; 301 Hz; 4.001 kHz.

Test setup: Connect distortion meter to output 34 MOD. GEN. and measure distortion with a load of 50 Ω and with a load of > 100 kΩ at above level and frequency settings.
Distortion should be ≤ 1%.

3.2.2.18.3 Checking the Accuracy of the Output Voltage

Settings: Frequency mod. gen. 1000 Hz.

Test setup: Connect AF voltmeter (10 Hz < frequency range > 25 kHz), input impedance ≧ 100 kΩ) to output MOD. GEN.

Set following levels on modulation generator and check using AF voltmeter:

5000.0 mV	6.4 mV
2560.0 mV	3.2 mV
512.0 mV	1.6 mV
51.2 mV	0.8 mV
25.6 mV	0.2 mV
12.8 mV	0.1 mV
	0.0 mV

Checking the frequency response:

Settings: Level mod. gen. 1000 mV.

Same test setup as above.

Set several frequencies between 10 Hz and 25 kHz on SMFP2 and check using AF voltmeter.

Total error (absolute value, frequency response, setting accuracy) must not exceed ±2% +0.1 mV.

3.2.2.19 Checking the RF Frequency Meter

3.2.2.19.1 Checking the Input Level Range at the Input FREQ. METER

Apply RF signal with a 10-mV level (into 50 Ω) to socket 47 FREQ. METER on front panel. Press key 46 FREQ. METER and check read out on frequency meter at 1, 10, 100, 200, 300, 400 and 520 MHz (if the SMFP-B2 1-GHz Frequency-range Extension Option is fitted, check also at 600, 700, 800, 900 and 1000 MHz).

Repeat at an input level of 1000 mV (into 50 Ω).

The internal RF synthesizer can be used for this check.

NOTE: If the frequency drops below the lower limit value or exceeds the upper limit value by even a slight account, the frequency meter will cease to give a readout.

3.2.2.19.2 Checking the Input Power Range at the RF Input/Output Socket

Apply 700-mV RF signal corresponding to an input power of 10 mW = 10 dBm to RF input/output socket 48 on front panel. Press key 49 TR. and check readout on frequency meter at 1, 10, 100, 200, 300, 400, 520 MHz (if the SMFP-B2 1-GHz Frequency-range Extension is fitted, check also at 600, 700, 800, 900, 1000 MHz). Checking at the maximum input power of 30 W is not necessary since the same signal paths are used for the counter control as for the FREQ. METER input. They merely differ in sensitivity.

NOTE: If the frequency drops below the lower limit value or exceeds the upper limit value by even a slight amount, the frequency meter will cease to give a readout.

3.2.2.19.3 Checking the Counter Accuracy

Apply to socket 47 FREQ. METER on front panel an RF signal with f > 500 MHz and a given frequency accuracy (check by means of external counter with an accuracy of 1 part in 10^{-9}) and a level of 10 mV < V < 1 V. Press key 46 FREQ. METER. The frequency readout must be within the accuracy of the master crystal.

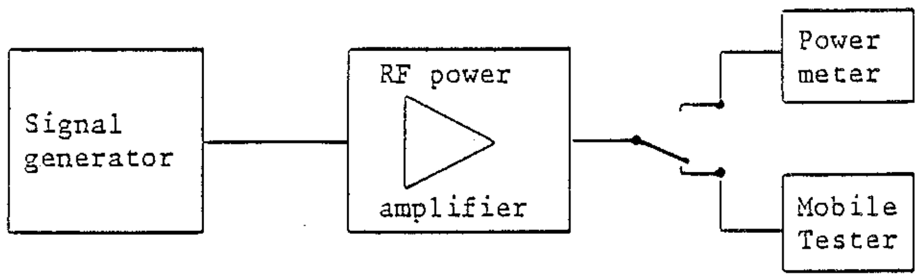
Adjustment: See section 5.4.2 a) or, if the SMS-B1 Option is fitted, 5.4.2 b).

3.2.2.20 Checking the Power Meter

Settings: Press keys 49 TR. and 50 FM.

In order to achieve the measurement accuracy guaranteed in the data sheet, it may be necessary to fit the coaxial 50-Ω resistor, which is supplied with the instrument, to rear socket 54.

Test setup:



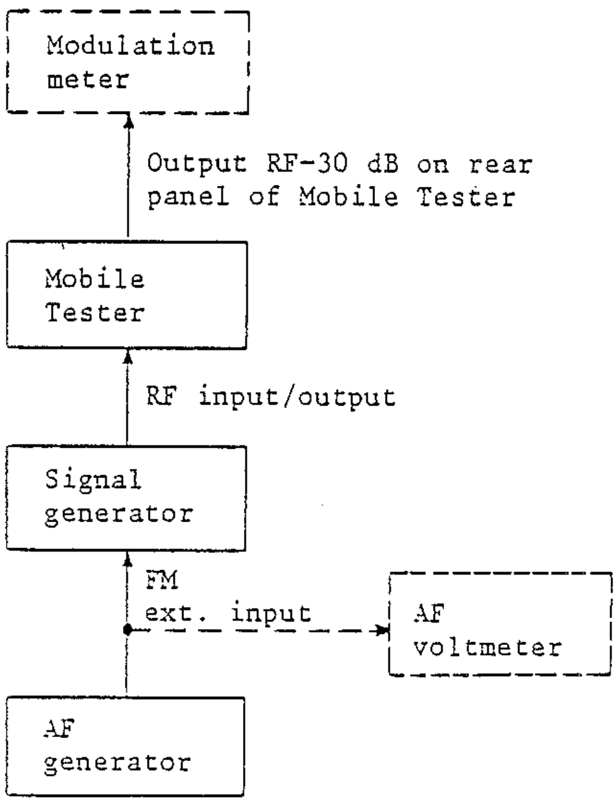
Feed in unmodulated power levels of 10 mW, 2 W and 30 W at 1 MHz, 30 MHz (and 1 GHz). Compare readout on display 5 of Mobile Tester with that on power meter.

The maximum permissible error is ±5% +1 digit and at f > 500 MHz ±10% +1 digit.

The power meter measures the unmodulated carrier power even if AM is present.

3.2.2.21 Checking the Frequency Deviation Meter

Test setup:



Checking the reading accuracy

Press keys 49 TR. and 50 FM on front panel and apply to RF input/output socket 48 signal derived from signal generator operating in power range 100 mW to 30 W and supplying a frequency of about 18 MHz. Feed to FM EXT. socket of signal generator an AF signal of 1 kHz and 1 V level and adjust modulation on signal generator such that modulation display 9 reads out a deviation of 20.0 kHz. Connect modulation meter to RF output socket on rear panel of Mobile Tester (RF 30 dB) and check reading accuracy. Subsequently reduce modulation of signal generator by reducing modulation voltage of AF generator and determine interdependency between deviation read out on Mobile Tester and modulation voltage.

Error of frequency deviation indication must not exceed ± (3% + 1 digit) down to 1 kHz.

3.2.2.22 Checking the Phase Deviation Meter

Test setup: Same as for checking frequency deviation meter (see section 3.2.2.21).

Settings: Press keys 49 TR. and 50 φM.

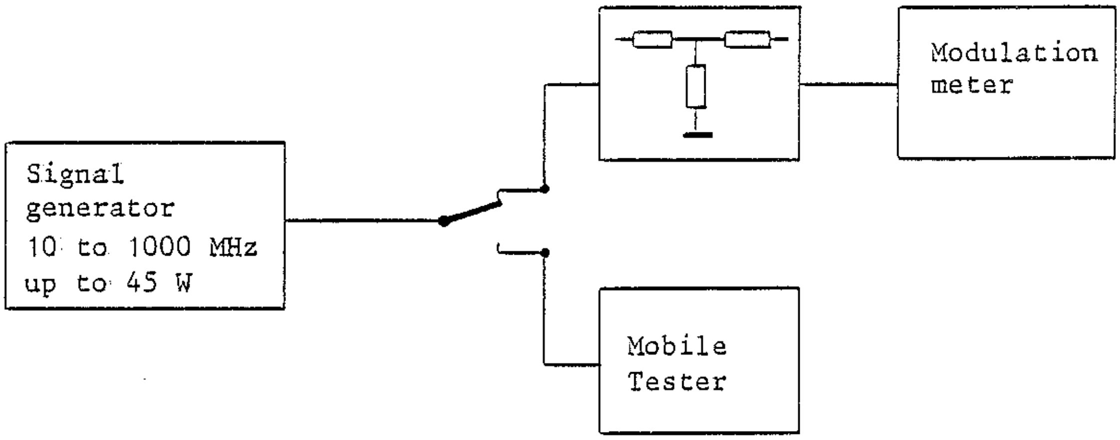
Apply to RF input/output 48 signal derived from signal generator operating in power range 100 mV to 30 W and supplying a frequency of about 18 MHz.
Feed AF signal of exactly 1 kHz and 1 V level to external socket of signal generator and adjust modulation on signal generator such that Mobile Tester reads out a phase deviation of 5.00 rad. Connect modulation meter to RF output socket on rear panel (RF 30 dB) and check reading accuracy. Make same test at 300 Hz and 3 kHz.

AF frequency response error occurring in addition to error of the frequency deviation meter should not be > ±2%.

3.2.2.23 Checking the Modulation Meter

Settings: Press keys 49 TR. and 50 AM.

Test setup:



Measure at test points listed in following table:

m = 0.8		AF	
Carrier powers	300 Hz	1 kHz	10 kHz
100 mW, 30 W			
20 MHz	±5% + 1 dg + F	±5% + 1 dg + F	±5% + 1 dg + F
RF 100 MHz	±5% + 1 dg + F	±5% + 1 dg + F	±5% + 1 dg + F
1000 MHz	±10%+1 dg + F	±10%+1 dg + F	±10%+1 dg + F

1 dg + F: 1 digit + RF frequency response

RF frequency response: ±4%

Permissible errors are given in the table.

3.2.2.24 Checking the DC Voltmeter

Settings: Press keys 51 REC. and 30 U/I DC once.

Feed a DC voltage, monitored by a digital voltmeter, with negative connected to chassis into banana socket 28 provided for this purpose.

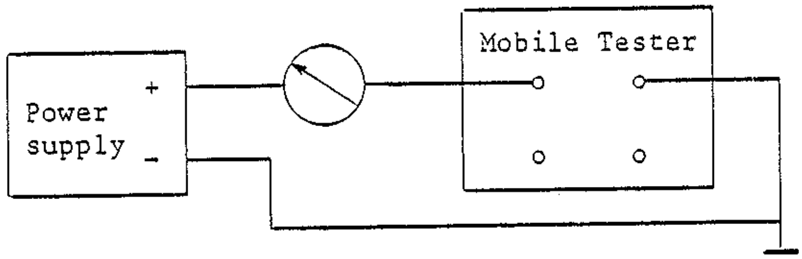
Measure at +10 mV, +3 V and +30 V.

The permissible error is ± (2 % + 2 digits).

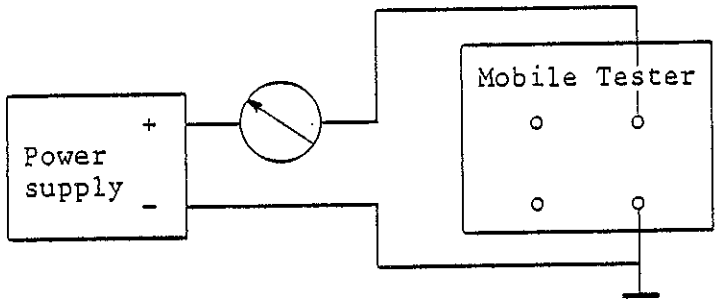
3.2.2.25 Checking the DC Ammeter

Settings: Same as for checking the DC voltmeter. Press key 30 U/I_{DC} twice.

Test setup:



Current range I



Current range II

Measure on current range I at 10 A and 200 mA. On current range II measure at 200 mA and 10 mA.

The measurement error must not be greater than ±(3% + 3 digits).

3.2.2.26 Checking the AF Level Meter

3.2.2.26.1 Checking the Frequency Response

Feed AF signal with a level of about 900 mV (permits measurement with highest possible resolution) to AF meter socket 31 on front panel. Press key 15 for AF level measurement and determine frequency response of AF level meter over frequency range from 50 Hz to 20 kHz.

3.2.2.26.2 Checking the Reading Accuracy as a Function of the Input Level

Feed 1-kHz AF signal to AF meter socket 31 on front panel. Press key 15 for AF level measurement and determine reading accuracy of AF level meter over input level range from 1 mV to 10 V.

The additive error must not exceed ±3% +1 digit. If, at certain input levels, the reading error is the same at all frequencies, adjust by means of R52 and R53 in DC amplifier. Frequency response error cannot be corrected.

3.2.2.27 Checking the AF Frequency Meter

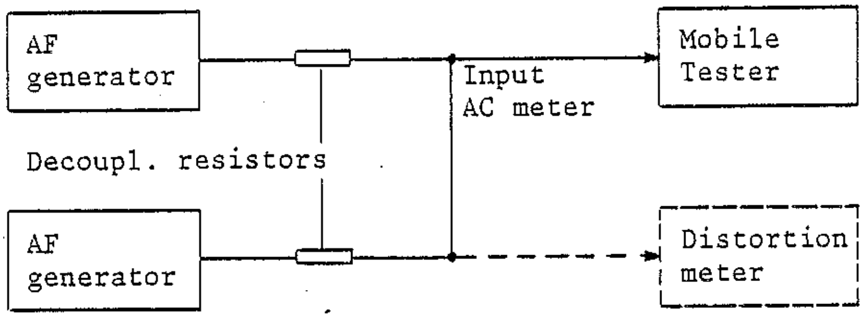
Feed AF signal within frequency range 20 Hz to 1 MHz, preferably at 20 Hz, 100 Hz, 1 kHz, 10 kHz, 100 kHz and 999,9 kHz, to AF meter socket 31.
Press key 33 EXT. NF/AC and determine sensitivity of AF counter. It should be < 10 mV. Subsequently check counter readout at an input level of 10 V and frequencies 20 Hz, 20 kHz and 999.9 kHz.

The counter sensitivity can be adjusted using R3 in the AF amplifier.

NOTE: If the upper cut-off frequency is exceeded even by a small amount, no readout will be obtained on the frequency meter.

3.2.2.28 Checking the Distortion Meter

Test setup:



Combine output signals of two AF generators via decoupling resistors and feed to AF meter socket 31. Adjust frequency of one AF generator exactly (±1%) to test frequency (1 kHz, 500 Hz, 300 Hz) and frequency of second AF generator to frequency of 2nd or third harmonic. Different output voltages of the two AF generators permit any desired distortion factors to be produced at the input of the Mobile Tester. If output attenuators of AF generators are not of adequate precision and inherent distortion is > 0.1%, distortion of test signal must be measured with an external distortion meter.

Press keys 15 EXT. NF/AC and 18 DISTORTION at 1 kHz, 500 Hz, 300 Hz.
Set distortion factors from 50% to 0.3%, preferably 50%, 10%, 3%, 1% and 0.3%, as described above, at various input levels within the measurement range.
Reading accuracy of distortion meter must be within ±5% +1 digit.

Finally, to check lower reading limit, apply a low-distortion (< 0.1%) 1-kHz, 500-Hz or 300-Hz signal with a 100 mV level and determine lower reading limit of distortion meter. It should be < 0.3%.

Adjustment: Adjust distortion meter by means of R17, R18, R30, R5, R67, R68, R72, R73, R96, R97, R116 and R117 on filter board (see section 5.5.6.2).

3.2.2.29 Checking the SINAD Meter

Test setup and measurement as for checking distortion meter. Press key 0 on keyboard 25 and key 19 for SINAD ratio measurement. Check reading accuracy of SINAD meter. Deviation from the nominal value must not be greater than ±1 dB.

NOTE: Frequency of the wanted signal should be 1 kHz. 300 Hz, as used for distortion measurements, is not permissible.

3.2.2.30 Checking the Interface Functions

Connect a controller to SMFP2. Program all setting instructions listed in section 2.3.5 and check proper execution of instructions by SMFP2 on front panel displays.

3.2.2.31 Checking the Adjacent-channel Power Meter Option SMFPB61

Test setup:

Connect signal generator to socket 48 and apply 20 mW in the frequency range between 10 and 520 MHz (amplitude-modulated signal, 2% modulation depth, modulation frequency 10 kHz, 12.5 kHz, 20 kHz or 25 kHz).

Settings on the Mobile Tester:
Enter modulation frequency of the signal generator in kHz via the keyboard 25 and store with one of the keys 2.

Enter the RF frequency of the signal generator in MHz via the keyboard 25 and store with key 3.

Call up adjacent-channel power measurement by means of NKL dB key 43.
The result (sideband of 2% amplitude-modulated signal = down 40 dB) is read out on the display 5. The permissible error is ±3 dB.

If the adjacent-channel power measurement is called up by means of the µW key 43, the result read out on display 5 is 2 µW. The permissible error is ±3 dB plus the error of the power meter.

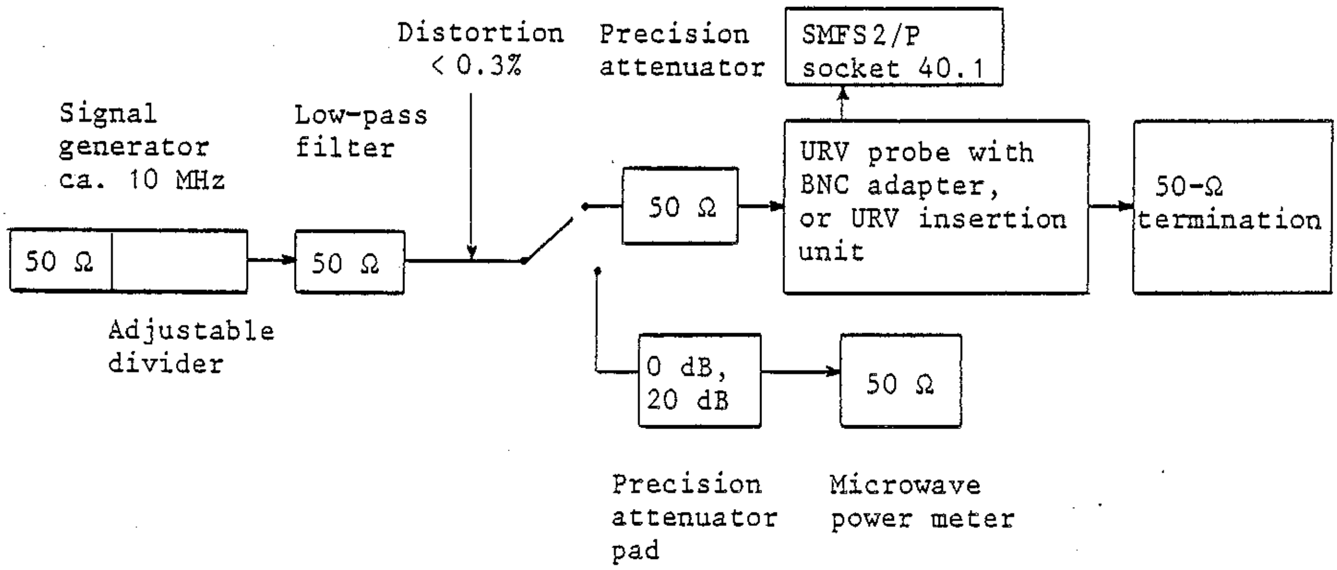
3.2.2.32 Measuring Accuracy of the RF Millivoltmeter Option SMFS2B8

NOTE: The option reaches the guaranteed performance specifications after a warm-up period of 10 minutes.

Since the test signal is processed in the measuring head, the measuring accuracy depends to some degree on the measuring head used. An appreciable indicating error may be caused by a fault in the option itself or in the measuring head. At any rate, a correctly operating measuring head must be used for checking the measuring accuracy.

Prior to measuring, calibrate the power meter with DC voltage. To this end, the power meter must be DC coupled.

Test setup:



At a signal generator frequency of about 10 MHz chose the amplitude of the signal generator such that the power meter indicates exactly 20 mW at the precision attenuator and attenuator pad settings given in the table below (calibration).

After switching over the signal path determine the deviation of the reading on the RF Millivoltmeter from the nominal value.

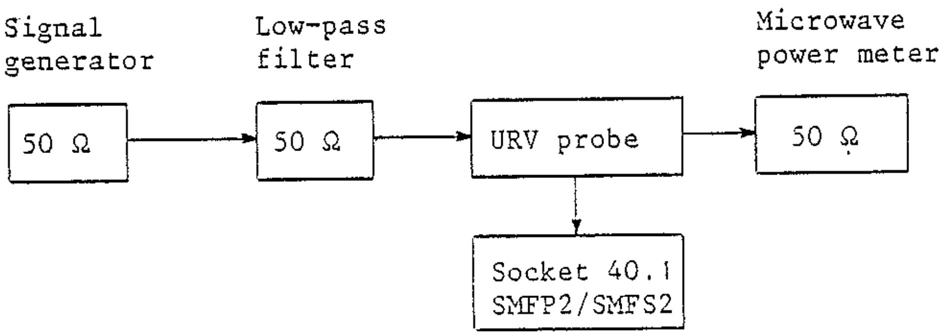
Calibration				Determination of measuring accuracy	
Signal general voltage	Attenuator setting	Precision attenuator pad setting	Reading on power meter	Nominal reading on RF Millivoltmeter Option	Max. deviation from nominal reading
10 V	0 dB	20 dB	20 mW	10 V	±(4% +6 digits)
10 V	20 dB	0 dB	20 mW	1 V	±(4% +6 digits)
10 V	40 dB	0 dB	20 mW	100 mV	±(4% +6 digits)
10 V	60 dB	0 dB	20 mW	10 mV	±(4% +6 digits)

3.2.2.32.1 Measurement of Frequency Response of Probe

NOTE: Particular care should be taken when measuring the frequency response on account of the bandwidth and sensitivity of the RF Millivoltmeter Option. Short, matched connections are very important.

Since the frequency response of the URV measuring heads is exclusively determined by the built-in measuring diodes and the mechanical construction of the measuring head, the frequency response need only be checked after the measuring head has been repaired.

Test setup:



Setup

- The ambient temperature must be between 20 and 25°C.
- Connect the probe to socket 40.1 and insert it into the BNC adapter.
- Calibrate the power meter with DC voltage.
- Apply an AC voltage to the BNC adapter with a frequency variable from 100 kHz to 1000 MHz and a distortion factor < 0.3%.

Performance check

Adjust the amplitude of the AC voltage so that it gives the same deflection on the power meter as a DC voltage of 1.000 V and keep it constant. Successively set the frequencies given in the following table and read off the value indicated on the display 5. The deviation from 1.000 V must not exceed the limits specified in the table.

Frequency/MHz	Max. permissible deviation from 1.000 V
0.1	±(4% + 6 digits)
1	±(4% + 6 digits)
100	±(5% + 6 digits)
200	±(8% + 6 digits)
500	±(10% + 6 digits)
1000	±(18% + 6 digits)

3.2.2.32.2 Measurement of Frequency Response of Insertion Units

The frequency response of the insertion units is best measured with the same test setup as under 3.2.2.32.1, but without precision attenuator and attenuator pad.

Setup

- The ambient temperature must be between 20 and 25°C.
- Connect the cable of the insertion unit to be checked to socket 40.1 and terminate the insertion unit at one end with the 50-Ω probe of a power meter.
- Calibrate the power meter with DC voltage.
- Apply an AC voltage to the insertion unit with a frequency variable from 1 kHz to 2000 MHz and a distortion factor < 0.3%.

Performance check

Adjust the amplitude of the AC voltage so that it gives the same deflection on the power meter as a DC voltage of 1.000 V and keep it constant. Successively set the frequencies given in the following table and read off the value indicated on the display 5. The deviation must not exceed the limits specified in the table.

Frequency/MHz	Max. permissible deviation from	
	1 V 10-V insertion unit	100 mV 100-V insertion unit
10 kHz	±(4% + 6 digits)	-
1 MHz	±(4% + 6 digits)	±(4% + 6 digits)
10 MHz	±(4% + 6 digits)	±(4% + 6 digits)
100 MHz	±(4% + 6 digits)	±(4% + 6 digits)
200 MHz	±(5% + 6 digits)	±(5% + 6 digits)
500 MHz	±(8% + 6 digits)	±(8% + 6 digits)
1000 MHz	±(10% + 6 digits)	±(10% + 6 digits)
1600 MHz	±(18% + 6 digits)	±(18% + 6 digits)
2000 MHz	±(18% + 6 digits) *)	±(18% + 6 digits)

*) Only with 50-Ω version.

4. Circuit Description

4.1 RF Generator Section

(See Fig. 4-25 in the appendix)

The output frequency of the SMFP2 is derived by frequency synthesis from a 10-MHz crystal reference source. The principal frequency-processing unit is the phase-locked loop of the two local oscillators 260 to 380 MHz and 380 to 520 MHz (PC boards Y3 and Y4). A reference frequency obtained by frequency addition in the functional group "mixer oscillator" (Y7) from the signals of the two interpolation oscillators (Y7, Y8) is fed to the phase detector of the functional group "local oscillators". One of the four fixed frequencies 300, 340, 420 ot 460 MHz is fed to the mixer in the feedback path of the phase-locked loop of the local oscillators (Y3). The fixed frequencies are obtained by mixing the signals of the two auxiliary oscillators, 80 MHz (or 40 MHz) (Y6) and 380 MHz (Y5).

The frequency of the signal in the feedback path of the phase-locked loops of the local oscillators at the phase detector input is given by

$$f = \left|(f_H - f_{osc})\right| \frac{1}{M}$$

where f_H is one of the four fixed frequencies and M is the division factor of the frequency divider. At synchronization, the frequencies of the two signals at the phase detector inputs are equal, i.e.

$$f_{ref} = \left|(f_H - f_{osc})\right| \frac{1}{M} .$$

Hence,

$$f_{osc} = f_H \pm M f_{ref} ,$$

where f_{ref} is the frequency derived from the interpolation oscillators. The oscillator frequency f_{osc} is constantly adjusted by the phase-locked loop so that this relation is fulfilled.

By addition of the two interpolation frequencies in the functional group "mixer oscillator" (Y7), the signal f_{ref} with a frequency of 2.0 to 2.2 MHz is obtained at the output of board Y7. This signal can be varied by varying the P divider in 100-Hz/M steps and the N divider in 50-kHz/M or 25-kHz/M steps.

The 50-kHz/M step size applies if $M > 19$ and the 25-kHz/M step size if $M \leqq 19$. The different step sizes are obtained because the 2:1 frequency divider connected in cascade with the M divider on Y6 is switched into circuit only for division factors $M \leqq 19$. The dependency of the step sizes on the division factor M is due to a frequency divider with the same division factor M as in the phase-locked loop of the local oscillators being connected ahead of the interpolation oscillators on board Y6. This ensures constant 100-Hz and 50-kHz step sizes of the oscillators independent of the division factor M.

Variation of the P and the N dividers of the interpolation oscillators permits the frequency of the local oscillators to be varied in 100-Hz steps over a range of 2 MHz.

The frequency division factor M is adjustable between 10 and 30. With each variation of M by one step, the frequency of the local oscillator is varied by a constant step size of 2 MHz over a range of 40 MHz .

The local oscillators are tunable in the frequency ranges f_H ±(20 to 60) MHz (f_H = one of the four fixed frequencies 300, 340, 420, 460 MHz) by setting the P, N and M frequency dividers accordingly.

Fig. 4.1 shows the relation between the four fixed frequencies, the division factor M and the frequency of the local oscillators.

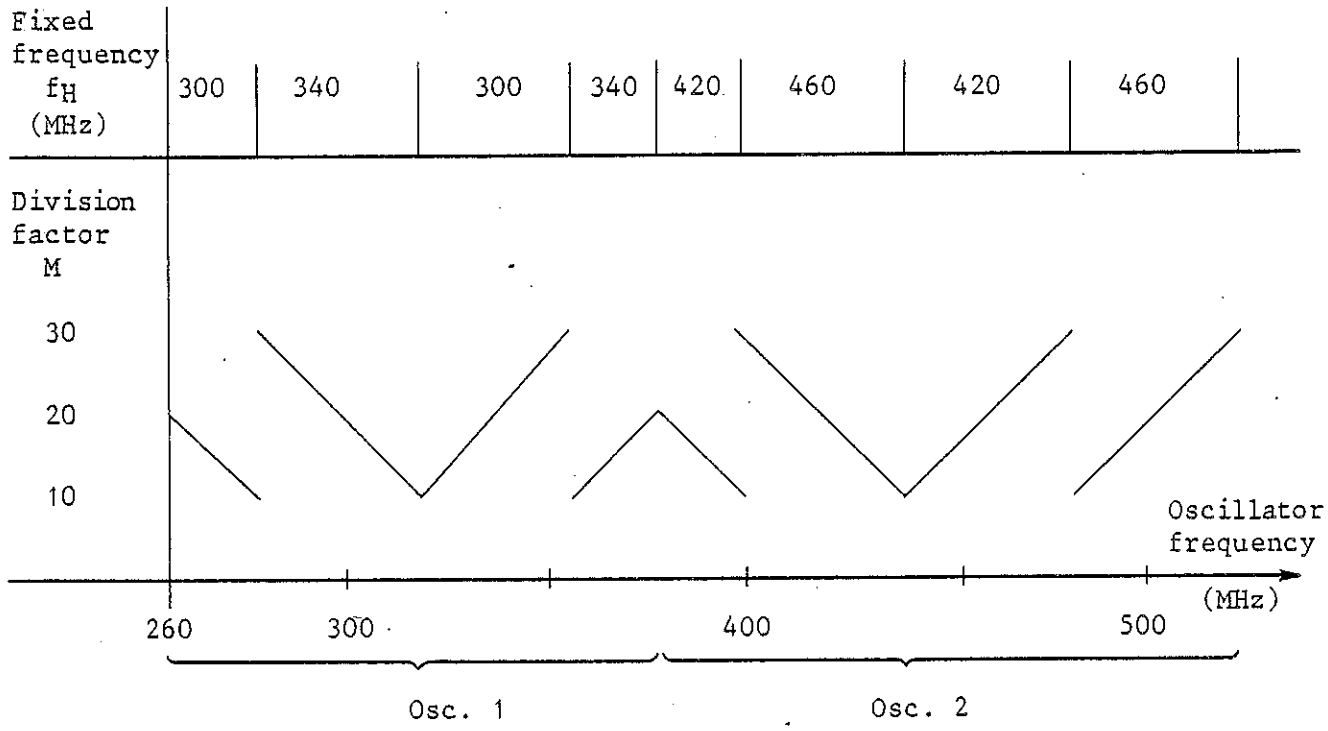


Fig. 4- 1 Relation between the four fixed frequencies, the division factor M and the frequency of the local oscillators

From 260 to 520 MHz, the output frequency of the SMFP2 is the frequency of the local oscillators. The range 130 to 260 MHz is produced on board 2 by halving the frequency. The output frequencies from 0.4 to 130 MHz are obtained by mixing with the 380-MHz signal on board Y1.

The functional group "fixed 80-MHz oscillator" (Y6) represents a phase-synchronized frequency modulator. With this type of modulator, the hold-in frequency of the phase-locked loop is far below the lowest modulation frequency. Thus synchronization is maintained even when the oscillator signal is modulated. The reference value for the modulation is produced on the board Y10 "modulation control". The modulation of the fixed 80-MHz oscillator is superimposed on the phase-locked loop of the local oscillators by means of the mixer.

Level control and amplitude modulation are combined in one control loop on the boards Y1 and Y2, the modulation signal being superimposed on the reference value of the level control. The reference value of the level control and the AM modulation signal are produced on the board Y10 "modulation control".

The output attenuator can be mechanically set in steps of 2 dB up to a maximum attenuation of 138 dB. The 0.1-dB steps are electronically set via the level control. The level control permits a total reduction of the RF level by 10 dB in steps of 0.1 dB, starting from a maximum level of +13 dBm.

All settings of the RF generator section are controlled by the microprocessor on board Y11. These settings include e.g. the setting of the M, N and P frequency dividers, the setting of the modulation and level attenuators on board Y10 for producing the reference values for modulation and level control, the setting of the output attenuator and switching of the local oscillators from 260 to 380 MHz and 380 to 520 MHz.

The microprocessor on Y11 is controlled by the computer board Y21.

4.1.1 Oscillator Y3

(See circuit diagram 302.5619 S)

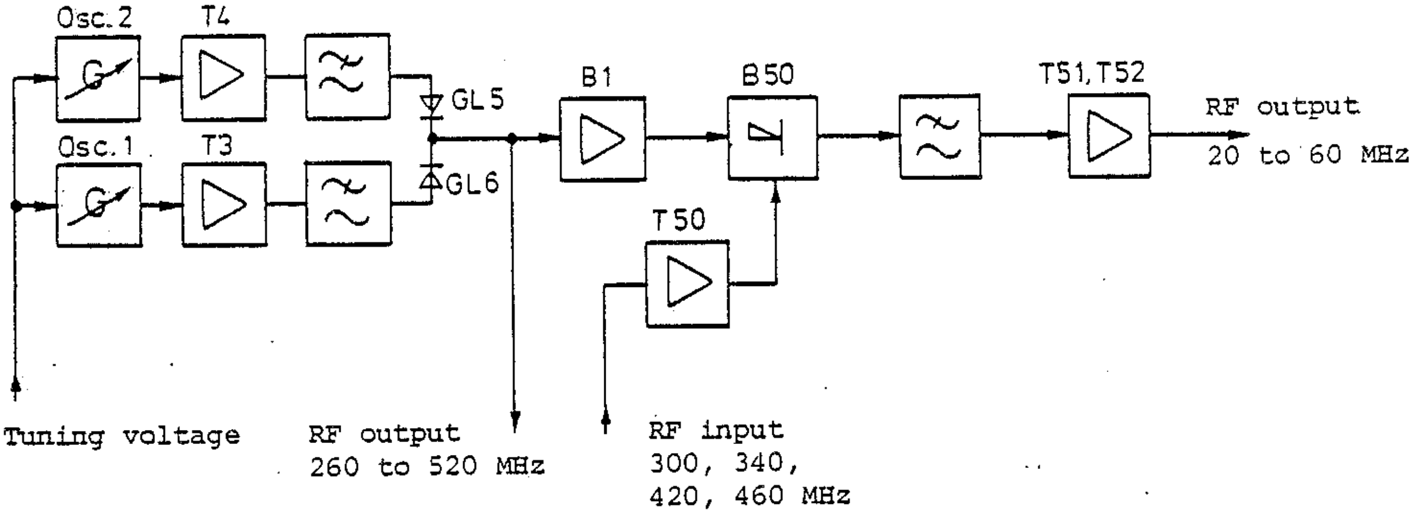


Fig. 4-2 Block diagram of the oscillator Y3

The oscillator unit Y3 contains two varicap-tuned RF oscillators. When one of the two is switched on, the other one is switched off. The frequency range of oscillator 1 is 260 to 380 MHz and that of oscillator 2 380 to 520 MHz. The two oscillator outputs are taken to the common output "RF output 260 to 520 MHz" via switching diodes.

The signal derived from the oscillator signal by conversion and available at the output "RF output 20 to 60 MHz" is taken to a phase detector for phase control of the oscillators. The phase detector and the associated phase control circuit are mounted on the phase control board. The functioning of the phase control is described in section 4.1.2.

Both oscillators, which operate on the negative impedance principle, use a FET as the active device. A varicap-tuned (GL1, GL2) inductance (L5, L6) is connected in parallel with the gate terminal. The oscillation characteristics are dependent on the drain current. The optimum operating point is set by means of the potentiometers R1, R2. The oscillator signal is fed out via the coils L7, L8.

The level is boosted by 6 dB in the subsequent amplifier stages (T3, T4), which are also used for decoupling. The following lowpass filters enhance the suppression of harmonics of the oscillator signal to 40 dB.

Ths oscillators and amplifier stages are switched on and off via the transistors T5, T7, which connect the oscillators to the +20-V supply voltage. The transistors T5, T7, in turn, are switched by means of a TTL signal at the oscillator switchover input 2b. If the input 2b is at "low" level, the oscillator 1 is switched on, T7 and switching diode GL6 are conducting, and T5 and switching diode GL5 are cut off. If the input 2b is at "high" level, the oscillator 2 is switched on, T5 and switching diode GL5 are conducting, and T7 and GL6 are cut off.

The tuning voltage for both oscillators is applied via a common line.

The signal level at output 4a, b "RF output 260 to 520 MHz" is between -2 dBm and +4 dBm. The suppression of harmonics is approximately 40 dB.

The integrated broadband amplifier B1 is high-impedance coupled to the "RF output 260 to 520 MHz". The amplifier output signal boosted to 4 dBm is available at the local oscillator input of the mixer B50. One of the fixed frequencies (300, 340, 420 or 460 MHz) is present at the RF input of the mixer. The signal level at the "RF input 300, 340, 420, 460 MHz" is about -20 dBm. It is boosted by 6 dB in the amplifier stage T50.

Utilizing both conversion sidebands, a signal between 20 and 60 MHz is obtained at the mixer output. A lowpass filter with a cutoff frequency of 70 MHz removes unwanted mixer products. The level of the signal at the "RF output 20 to 60 MHz" is about 0 dBm.

4.1.2 Phase Control Board Y4

(See circuit diagram 302.5890 S)

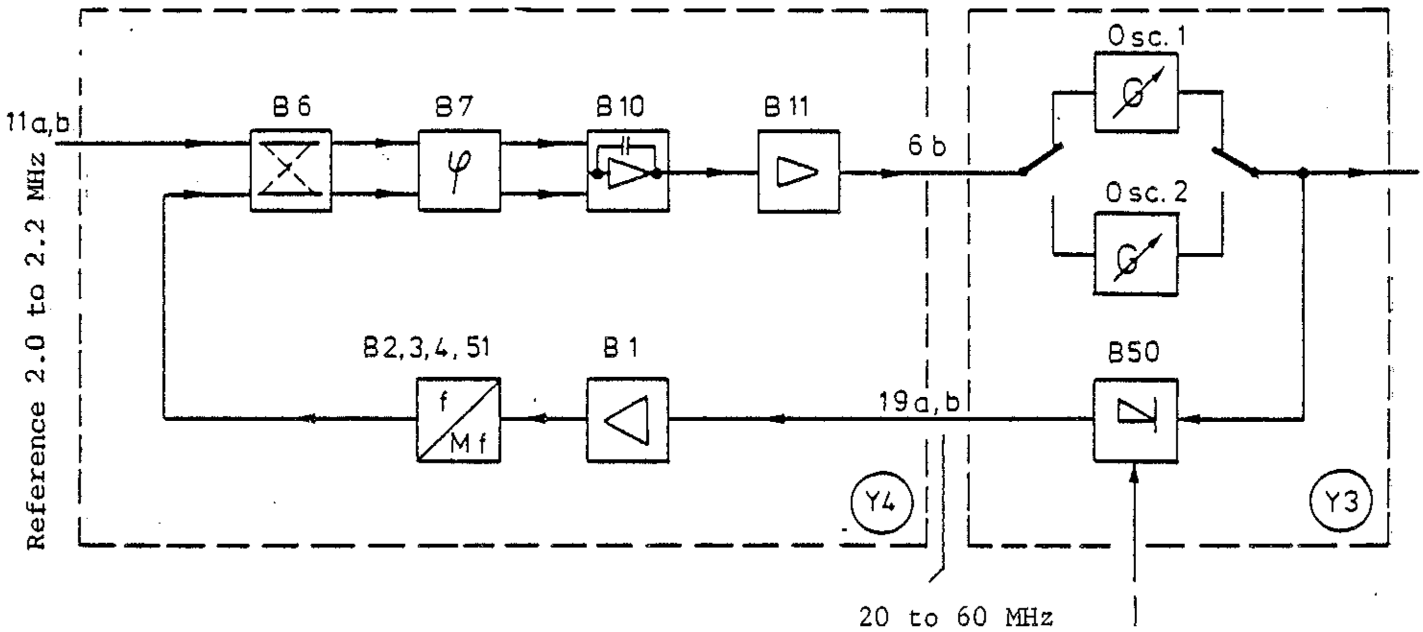


Fig. 4-3 Block diagram of the phase control loop

The phase control board together with the oscillator board forms a phase-locked loop holding local oscillators 1 and 2 in phase synchronization with the reference frequency derived from the two interpolation oscillators.

The oscillator signal is converted down to between 20 and 60 MHz in the mixer B1 in the feedback path of the control loop. Frequency division by the factor M is accomplished in the M divider which is also in the feedback path. M is adjustable to between 10 and 30. At synchronization, both input signals at the phase detector B7 are of equal frequency. The pulse-shaped output signals of the phase detector are applied to the integrator B10 which produces the control voltage. The tuning voltage for the two local oscillators is formed from the control voltage and a fixed DC voltage in the summing amplifier B11.

For the frequency ranges 260 to 320 MHz and 380 to 440 MHz, the frequency available at the output of the M divider is $(f_H - f_{osc})$: M and for the frequency ranges 320 to 380 MHz and 440 to 520 MHz it is $(f_{osc} - f_H)$: M.

Hence when changing the oscillator frequency, in one case the change in frequency at the divider output is in the same direction and in the other case in the opposite direction. In order to obtain the correct direction for the lock-in of the control loop in both cases, the inputs of the phase detector B7 are reversed by the gate B6.

When the control inputs 10, 12 of B6 are at low/high levels, the input 9 is connected through to the output 15 and input 4 to output 2. When the control inputs 10, 12 are at high/low levels, the input 9 is connected through to the output 2 and the input 4 to the output 15.

The M divider consists of the two programmable counters B2 and B3, the gate B51 for decoding the counter outputs, and the latch flipflop B4. The counters operate as down-counters, i.e. they count from the preset figure M corresponding to the bit pattern present at the data inputs D_0 to D_3 down to zero.
The division factor is present at the data inputs in binary code, the least significant bits (LSB) being allocated to B2 and the most significant bit (MSB), which is 2^4, to B3. Every positive-going edge of the clock signal decrements the counter. When the counter B2 has reached the count 0000, the carry output C OUT goes "low" for one clock period. The carry is carried over to the following counter B3 via the input C IN, the counter B3 being decremented by 1 with each carry. The condition for presetting the counter is decoded from the bit pattern present at the counter outputs Q_0 to Q_3 of B2 and B3 two clock pulses prior to reaching the count 0000. The pulse trains thus obtained with the divider preset for a division factor of 12 are shown in Fig. 4-4.

The control inputs S1 are "high" during the count phase. When the count 2 is reached, the D input of flipflop B4 goes "high". With the next clock pulse, the "high" signal is transferred to the flipflop and, as a result, the control inputs S1 and the D input go "low". The next clock pulse sets the counter and applies a "low" signal to the flipflop, so that the control inputs S1 again go "high" and the count cycle is restarted.

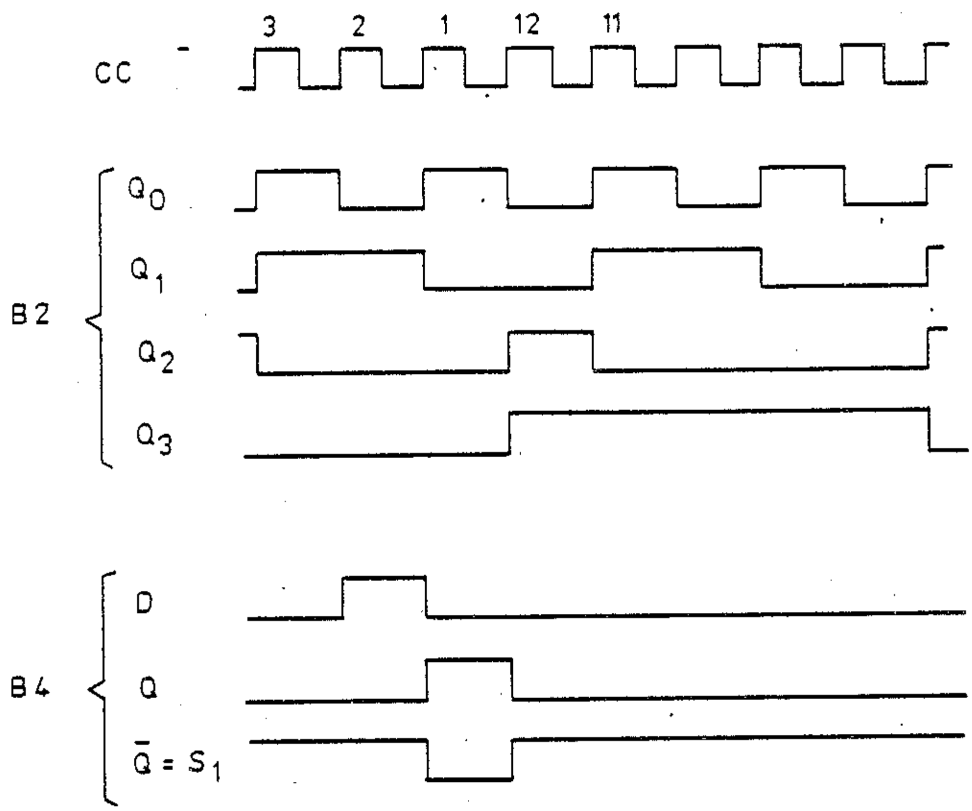


Fig. 4-4 Pulse train of the counter outputs Q_0 to Q_3

Line amplifier B1 connected ahead of the frequency divider amplifies and converts the 20-to-60-MHz input signal to ECL level.

The digital phase detector B7 is an edge-triggered flipflop. Triggering is accomplished by the positive-going edges of the signals at the inputs 6 and 9. The outputs 3 and 12 supply pulses, the duty cycle of which depends on the phase or frequency difference of the two input signals. If the frequency of the two input signals differs, the integrator voltage across C43 is corrected by means of the output pulses of the phase detector until the frequencies of the two input signals at the phase detector input are equal. When the frequencies are equal, the integrator is only pulsed sufficiently to ensure a constant integrator voltage.

The Schmitt trigger circuits B12I/II prevent the control loop from being blocked at the operating limits of the integrator B10 during the lock-in process.

The dynamic range of B10 is ±6 V. The switch-on thresholds of the Schmitt trigger circuits C12I/II are -12 V and +12 V respectively. The switch-off threshold of both Schmitt trigger circuits is 0 V. As soon as the output voltage of B10 reaches +12 V or -12 V, the Schmitt trigger B13/II or B12/I causes the diode GL4 or GL3 to conduct. The current through these diodes discharges the integrator to 0 V.

The resistive dividers R109/R111 to R113 and R109/R114 to R117 permit four fixed voltages per oscillator to be set. B19 and B20 each contain four FET switches. The switching information for the FET switches is obtained from the decoder B18 by the control signals A, B, C. The oscillator tuning voltage is produced in B11 by adding the fixed voltage and the control voltage from the integrator B10.

In order to keep the loop gain of the control circuit constant, the control voltage gain is altered. By switching over the resistors R143, 144, 145 - depending on the setting of the M divider - the gain variation due to the frequency divider in the feedback path of the control loop is compensated for. By switching over the resistors R94 to R98 - depending on the control signals A, B, C - the variation of the tuning sensitivity of the oscillators is compensated for.

The T-section resonant circuits connected in series with the amplifier B11 reject the 2-MHz and 4-MHz components of the tuning voltage originating from the 2-MHz frequency at the phase-detector input.

4.1.3 100-Hz Interpolation Oscillator Y8

(See circuit diagram 302.6615 S)

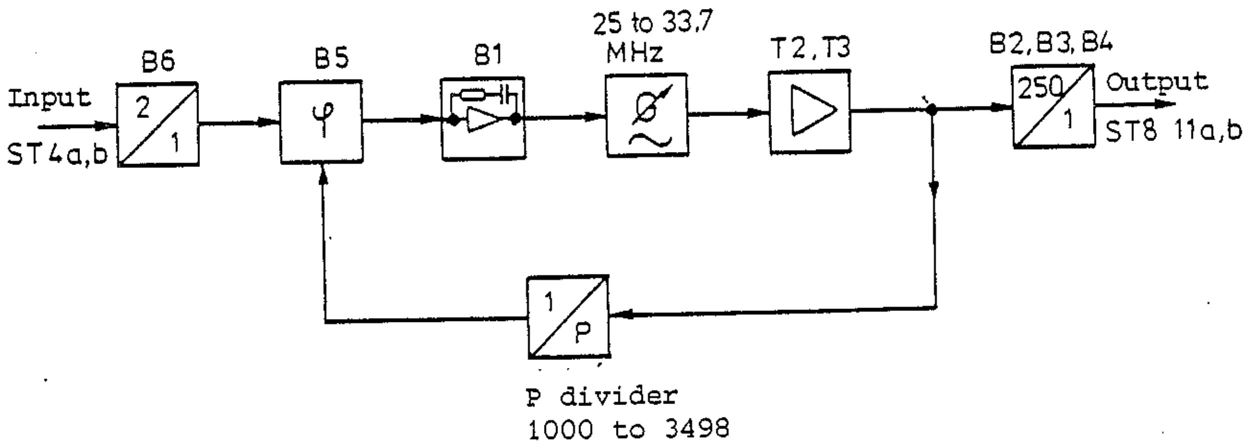


Fig. 4-5 Block diagram of the interpolation oscillator

The 100-Hz interpolation oscillator unit comprises a phase-locked loop with the programmable frequency divider P in its feedback path. The frequency at the output can be varied between 100 and 135 kHz with a frequency step width of 1/M kHz by variation of the division factor P. M equals the division factor of the frequency divider in the phase control loop Y4. The digital phase detector B5 is an edge-triggered flipflop with tri-state output. Triggering is accomplished by the positive-going edges of the signals at the signal input 14 and at the reference input 3. Output 13 supplies pulses with a voltage level "low" or "high" and duty cycle dependent on the phase and frequency difference between the input signals. If the frequencies of the two input signals differ, the integrator voltage across C1 is corrected by means of the output pulses of the phase detector until both signals at the phase detector have the same frequency. As soon as this is the case, C1 is charged only to the extent necessary to keep the integrator voltage constant. The oscillator is tunable through the range from 25 MHz to 33.7 MHz by the triple varicap GL3.

The P divider consists of three programmable counter ICs B7, B8, B9 and the latch flipflops B10. B7, B8 and B9, which are connected in cascade, operate as an asynchronous down-counter. The division factor is present in binary code at the 12 data inputs, the LSB being present at B9 and the MSB at B7. The borrow outputs of the counters B7 and B8 supply a negative pulse with a pulse duration corresponding to the input pulse at the count-down inputs as soon as the counters have reached the count 0000.

The borrow outputs of B7, B8 and the counter output Q_D of B9 are combined via an OR circuit. In this way, the condition for presetting the counters is decoded. As soon as the borrow outputs of B7, B8 and the Q_D output of B9 go "low", the flipflop B10 is enabled via the preset input. At the count 3, the counter output Q_D of B9 goes "low". With the next clock pulse, the "low" signal is transferred to the flipflop B10I.

At the count 1, the Q and $\overline{Q}$ outputs of B10/II go "low" and "high" respectively. A "low" signal is supplied to the load inputs of the counters, thus resetting the counters. The "high" signal present at the Q output of B10/II, resets B10/I via the preset input. After the load inputs have again gone "high", the new count cycle starts.

The data inputs to the counter ICs are set by the I/O expander B11. The setting data are read in at the input port P2, transferred to the output ports P4 to P7 and stored. The control signals E, F, G and H, the functions of which are listed in the Tables 4-1 and 4-2, are present at the output port P4.

Table 4-1

Control signal	HIGH	LOW	
E	Lowpass filter 260 MHz	Lowpass filter 190 MHz	Y2
F	Mixer on	Mixer off	Y1
G	Doubler on	Doubler off	
H	AM slow		Y1

Table 4-2

	0.4 to 5 MHz	5 to 130 MHz	130 to 190 MHz	190 to 260 MHz	260 to 520 MHz	520 to 1040 MHz
E	L	L	L	H	L	L
F	H	H	L	L	L	L
G	L	L	L	L	L	H
H	H	L	L	L	L	L

4.1.4 50-kHz Interpolation Oscillator Y7

(See circuit diagram 302.6415 S)

The output signal of the 100-Hz interpolation oscillator board Y8 is applied to the input ST7.11a, b. The frequency 500/M (kHz) for M > 19 or 250/M (kHz) for M $\leqq$ 19 is applied to the input ST7.4a, b, M being the division factor of the frequency divider of Y4. The programmable divider N is connected in the feedback path of the phase-locked loop of the 50-kHz interpolation oscillator. The division factor N permits the frequency of the 50-kHz interpolation oscillator to be varied in steps of 500/M (kHz) or 250/M (kHz).

The frequencies of the 100-Hz interpolation oscillator (Y8) and of the 50-kHz interpolation oscillator (Y7) are added in the phase-locked loop of the mixer oscillator. The sum frequency equals the frequency of the mixer oscillator.

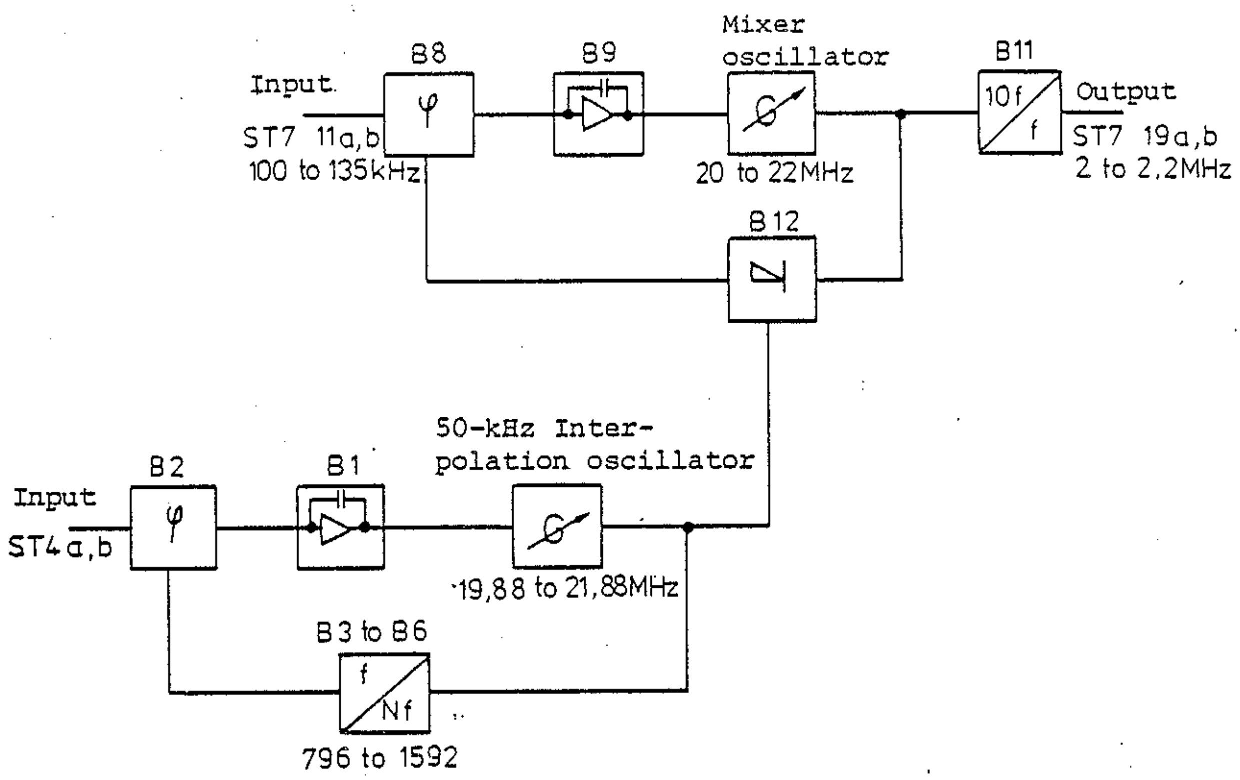


Fig. 4-6 Block diagram of the 50-kHz interpolation oscillator Y7

The digital phase detectors B2 and B8 are edge-triggered flipflops with tri-state outputs. Triggering is accomplished by means of the positive-going edges of the signals at the signal input 14 and at the reference input 3. Output 13 supplies pulses with a voltage level (low or high) and duty cycle dependent on the phase or frequency difference of the input signals.
If the frequencies of the two input signals differ the integrator voltage at C1 or C11 is corrected by means of the output pulses of the phase detector until the two signals at the phase detector have the same frequency. As soon as this is the case, the integrator capacitors are recharged only to the extent necessary to keep the integrator voltage constant. The integrator voltage serves as the oscillator tuning voltage.

The Schmitt trigger circuit B10 prevents the control loop from being blocked at the lower operating limit of the integrator B9 during the lock-in process. As soon as the tuning voltage drops below the response threshold of the Schmitt trigger circuit (4 V), the integrator is recharged to the maximum tuning voltage (25 V) via the diode GL10.

The divider N consists of three programmable counters B4, B5 and B6 connected in cascade and the latch flipflop B3. The counters operate as down-counters. The division factor is present in binary code at the 12 data inputs, the LSB being present at B6 and the MSB at B4. At the count 0000, the borrow outputs of B4 and B5 supply a negative pulse which has the same pulse width as the input pulses at the count-down inputs.

The borrow outputs of B4, B5 and the counter outputs Q_A, Q_C and Q_D of B6 are gated via an OR circuit. In this way, the condition for presetting the counters is decoded.

As soon as B4 and B5 have reached their final count and B6 the count of 2, the D input of the flipflop B3 goes "low". With the next positive-going clock edge, the "low" signal is transferred to the flipflop. While a "low" signal is present at the load inputs, the counters are reset. With the next positive-going clock edge, the "high" signal of the Q output fed back to the D input is transferred to the flipflop. The next positive-going clock edge starts the countdown from the new counter state.

The data inputs of the counters are set by the I/O expander B13. The setting data are read in at the input port P2, transferred to the outputs ports P4, P7 and stored.

The control signals A, B, C, D (A, B: range identification, C: oscillator switching, D: divider switching) are present at the output port P4.

Table 4-3

A	B	C	Frequency range (MHz)	Oscillator Y3
L	L	L	260 to 280	260 to 380 MHz
H	L	L	280 to 320	260 to 380 MHz
L	H	L	320 to 360	260 to 380 MHz
H	H	L	360 to 380	260 to 380 MHz
L	L	H	380 to 400	380 to 520 MHz
H	L	H	400 to 440	380 to 520 MHz
L	H	H	440 to 480	380 to 520 MHz
H	H	H	480 to 520	380 to 520 MHz

	0.4 to 130 MHz	130 to 260 MHz	260 to 1040 MHz
D	L	H Divider on Y2	L

4.1.5 Converter Y5

(See circuit diagram 302.6015 S)

A 380-MHz signal (ST5.19ab) and a conversion frequency 300, 340, 420 or 460 MHz (BU14) are produced on the converter board Y5. The 380-MHz signal is used on the circuit board Y1 as mixer signal for conversion of the range 380.4 to 510 MHz to the output frequency range 0.4 to 130 MHz. From the conversion frequency, the IF for the phase control is obtained on the PC board Y4 by mixing it with the signal of the main oscillator.

The 380-MHz signal is produced by an oscillator, the output signal of which is divided to 1 MHz by 380:1 frequency division and which is synchronized by means of a phase comparison circuit with the 1-MHz reference frequency available at ST5.15a. Using the upper or the lower sideband, the four conversion frequencies are obtained by mixing the 380-MHz signal with the reference frequency of 40 or 80 MHz applied to ST5.11a,b.

The 380-MHz oscillator is based on the FET T1. The elements of the tuned circuit are L3, C3, C4, C7 to C10 and the tuning diode GL1. The oscillator voltage is output via L3 and boosted by about 10 dB in a two-stage amplifier (T2 to T3). A resistive branching network (R13 to R16) is connected between the first and the second amplifier stages, via which the 380-MHz signal is output (ST5.19a,b). Likewise a branching network (R23 to R31) is connected to the output of the second amplifier stage, via which the signal passes to a 10:1 ECL divider (B1). The 38-MHz output signal of this divider is converted to TTL level in a level converter (T5-T6). Subsequently, the frequency is again divided, first in a 2:1 divider (B2/III) and then in a programmable divider circuit (B3 to B4) with fixed division ratio 19:1. The output signal of the divider - after division from 380 MHz to 1 MHz - is taken to a phase discriminator (B5), at whose reference input the 1-MHz signal from ST5.15a is present. The pulses delivered by this phase discriminator are integrated after phase comparison by means of a differential integrator (B6) to give a DC voltage which, after removal of the reference frequency by means of a lowpass filter (R46-R47-C49), is supplied to the varicap GL1 as tuning voltage. Tuning voltage control ensures that the two 1-MHz signals at the phase discriminator are always in phase. The operating point of the tuning voltage can be adjusted by means of the trimmer C9.

The conversion frequency is obtained by taking the 380-MHz signal from the second output of the branching network R22 to R26, boosting it in an integrated RF amplifier (B10) to about 5 dBm and applying it to the mixer B11 as mixer signal, where it is mixed with the 40- or 80-MHz reference signal present at ST5.11a,b. As a result, the frequencies 340 MHz and 420 MHz or 300 MHz and 460 MHz are obtained. Since the conversion frequency must be of high spectral purity (level of non-harmonic spurious signals > 70 dB down), it is always necessary to suppress one of the sideband frequencies developed during mixing. This is accomplished by means of four two-circuit-bandpass filters tuned to 300 MHz (L26-L27), 340 MHz (L20-L21), 420 MHz (L24-L25) and 460 MHz (L22 to L23). By means of switching diodes (GL10 to GL27) connected to the inputs and outputs of the filters, one filter is switched on while the remaining three remain cut off. The switching states are controlled by the signals present at ST5.13b and 15b via the switching stage comprising B12, and T8 to T11.

4.1.6 Reference Board Y6

(See circuit diagram 302.6215 S)

The frequency synthesis reference signals required for the interpolation oscillators on the circuit boards Y7 and Y8 and for the fixed 80-MHz and 380-MHz oscillators on the circuit boards Y5 and Y6 are produced on the reference board Y6.

All signals are derived from a 10-MHz oscillator. The 1-MHz signal is obtained by 10:1 frequency division. The 80-MHz signal is produced by an oscillator whose frequency is divided from 80 MHz to 10 kHz and synchronized with the crystal frequency which is also divided to 10 kHz. Changeover to 40 MHz is accomplished by 2:1 frequency division. The reference signals for the circuit boards Y7 and Y8 are obtained by frequency division of the 1-MHz signal by means of a divider programmable to between 10:1 and 30:1.

The 10-MHz crystal oscillator comprises transistor T10 with the crystal Q1 as selective feedback element between collector and emitter. C62 permits the oscillator frequency to be slightly varied. The output is fed out via a capacitive divider (C60-C61). By inserting BR1 to BR3 as appropriate, a temperature-compensated crystal oscillator (option) can be connected to pin 1, and at pin 4ab the internal reference can be brought out or an external reference frequency fed in.

The crystal oscillator is followed by a buffer amplifier (T6 to T8) and a 10:1 divider (B11). The 1-MHz signal from this divider is brought out at ST6.19ab and at the same time applied to a 100:1 divider (B10/I and II) via a buffer stage (T5). The 10-kHz output signal of the 100:1 divider is the reference frequency for the phase discriminator (B12) of the phase-locked loop of the 80-MHz oscillator.

The 80-MHz oscillator includes the FET T1 and the tuning elements GL1-GL2 (varicaps). The tuning voltage of the phase-locked loop is applied to GL1 which synchronizes the oscillator with 80 MHz. Frequency modulation is accomplished via GL2. The oscillator voltage is fed out via C9 and boosted to TTL level via the amplifier T2, T3. The signal then passes through a frequency divider chain (B5I 2:1, B5II 2:1, B6 10:1, B7 2:1, B8 100:1) in which it is divided from 80 MHz to 10 kHz and applied to the phase discriminator B3 for comparison. By integrating the pulses from the discriminator in integrator B13, a tuning voltage (MP1) is produced which maintains the comparison signal and the reference signal at the phase discriminator in the phase-locked condition.

Either 40 MHz or 80 MHz are required as reference at the output ST1/11ab depending on the frequency of the output signal of the equipment. The reference signal is derived either from the transistor T3 (80 MHz) or from the first frequency divider stage B51 (40 MHz). Switchover is effected by means of the gates B3/II and B4/IV and the switching diodes GL5 and GL6. In a lowpass filter for 40 MHz (L10 to L13-C22 to C24) and a lowpass filter for 80 MHz (L5 to L8-C18 to C20), the TTL signals are shaped into sinewave signals.

The frequency modulation is produced in the 80-MHz oscillator by means of the varicap diode GL2. To prevent the modulation from being eliminated by the phase control, the phase-locked loop has been slowed down by means of an RC section (R24-C12). The modulation voltage passes from ST6.13b via a switchable resistive divider to the varicap diode GL2. The frequency deviation of the oscillator is doubled by this resistive divider if the reference frequency is 40 MHz, since this passes through a 2:1 divider which halves the frequency deviation.
The deviation sensitivity is set by means of R9 (for 80 MHz) or R12 (for 40 MHz). The operating point of the oscillator is set by R7.

The deviation switch and the 40/80-MHz switch are controlled by gating of the switching signals at ST6.66 and .68 with the gates B1 and the amplifier B2.

The reference signal for the circuit board Y8 (ST6.66) is obtained by frequency division of the 1-MHz signal by means of a 2:1 divider (B14 /I) and the M divider connected in cascade. This divider consists of the ICs B14 to B16. The input signal is derived from the collector of T5. The division ratio is adjustable with a binary control signal to between 10 and 30 via the inputs ST6.13a, .15ab, .17ab. The output frequency thus obtained lies between 16.66 and 50 kHz.

From the reference signal for the circuit board Y8, the reference signal for the circuit board Y7 is produced (ST6.8a). It remains unchanged if the M divider setting > 19. If the M divider setting lies between 10 and 19, 2:1 frequency division will take place. For this purpose, a 2:1 frequency divider is provided (B17), which is switched on or off depending on the binary control signal of the M divider via a logic circuit (B18).

4.1.7 Divider Y2

(See circuit diagram 302.5419 S)

The divider board Y2 is connected into the RF signal path between the local oscillator (Y3) and the output stage (Y1). It comprises an RF switch, a 2:1 frequency divider and the amplitude modulator.

For output frequencies from 260 to 520 MHz, the signal from the local oscillator passes via the RF switch directly to the amplitude modulator and on to the output stage Y1. For output frequencies 130 to 260 MHz, the local oscillator still operates in the range 260 to 520 MHz, but its output signal is in this case taken to the modulator via the 2:1 frequency divider and then on to the output stage Y1.

Either the switching diodes GL1, GL3, GL6 and GL55 (without divider) or the switching diodes GL10, GL2, GL4 and GL56 (with divider) in the RF switch conduct; the other group is cut off. The RF switch is controlled via B3/I and the switching stage T70-T71. Together with the RF switch, the divider B1 is also controlled. Its supply voltage is switched on by T72 only when the frequency is to be divided.
The input signal to the divider is applied via GL10 and R11. The attenuator pad R10 to R12 match-terminates the local oscillator since input 1 of the

divider exhibits a high impedance. R13 influences the response threshold and consequently (to a minor degree) the input sensitivity. The divided output signal (contact 6 B1) is boosted by about 15 dB by means of an integrated RF amplifier (B2). Since this signal is almost rectangular, optimum suppression of harmonics is effected by means of the two cascaded lowpass filters. The upper lowpass filter in the circuit diagram is effective in the range 130 to 190 MHz and the lower one in the range from 190 to 260 MHz. The lowpass filters are switched in or out by means of the switching diodes GL20-GL21 and GL40 to GL42, respectively. The switching diodes are driven from B3/III.

The RF signal passes then to the amplitude modulator, which constitutes the control element for level control and amplitude modulation. The two integrated circuits B4 and B5 each contain three PIN diodes in π-connection. The required attenuation is set by the control voltage produced in the output stage, which passes via ST2.17b to the divider. The inherent attenuation of the modulator is about 8 dB. Before being fed to the output stage Y1 via ST2.19ab, the RF signal is boosted by about 15 dB in the broadband amplifier B6.

4.1.8 Output Stage Y1

(See circuit diagram 302.5219 S)

On the output stage board, the RF signal from the divider Y2 is boosted to 13 dBm, the maximum level available at the output of the set.

The signal passes via an RF switch directly to the final amplifier in the frequency range 130 to 520 MHz. The output frequency range 0.4 to 130 MHz is obtained by mixing the range 380.4 to 510 MHz with a signal of 380 MHz.

The RF detector for level measurement is located at the output of the final amplifier. The detected voltage is compared with a reference level in the control amplifier, the voltage thus obtained is the control voltage required for control of the amplitude modulator.

The RF switch consists of the switching diodes GL2 to GL6 for the direct path and GL1, GL8 and GL9 for signal flow via the mixer.

The input signal is applied to the mixer (B1) via a lowpass filter (C2 to C7, L1 and L2) and an attenuator pad (R1 to R3) connected in tandem. The balanced mixer is of printed circuit design. The frequency separation of the input signal and the output signal which are present at the same contact (3) is accomplished by means of a filter (C8 to C14; L3 and L5). The mixer signal (380 MHz) is applied via BU12 and is boosted to about 14 dBm in a tuned amplifier.

The trimmer C91 can be used to minimize non-harmonic spurious signals in the conversion range. The output signal of the mixer is taken to a two-stage amplifier (T1-T2) where it is boosted to about 0 dBm. The following lowpass filter with a cutoff frequency of 140 MHz is used for suppression of the mixer signal and of the non-harmonic spurious signals with frequencies above 140 MHz.

The RF switch and the 130-MHz amplifier are controlled from the switching stage B2/I-T5-T6. The amplifier is only connected to the supply voltage during the mixing process.

The RF signal passes next to the two-stage final amplifier where it is further boosted by about 17 dB. On account of the required minimum level of harmonics (down > 30 dB), the power dissipation in both stages is so high that additional cooling must be provided. This is mainly effected by the upper PC board cover. For this reason, the stage must not be operated without the cover over an extended period of time. R36 and R51 permit the collector currents to be adjusted so as to ensure minimum level of harmonics.

The detector diode GL12 connected before resistor R71, which acts as signal generator output impedance, is used for measuring the output level. The resulting detected voltage is applied to the non-inverting input of the control amplifier B5. By comparison with the reference level applied to the inverting input via R96, a control voltage is obtained (ST1.13b) which adjusts the attenuation of the amplitude modulator so that the detected voltage and the reference level are equal, i.e. the level before the network R71-R73-C72 acting as output impedance is kept constant. The signal generator thus functions as a voltage source with 50 Ω internal impedance.

Moreover, the detector circuitry provides frequency response compensation for the effects of RF attenuator and the connecting cables between the output of the final amplifier and the output of the set. L22, R60 and R61 are effective between 0.4 and 20 MHz and R73 with C72 between 20 and 150 MHz. The compensation in the range 200 to 500 MHz is adjustable by means of C64.

The value of filter capacitor C66 permits the detected voltage to follow an amplitude modulation up to about 25 kHz. For carrier frequencies below 5 MHz the capacitance of the filter capacitor is increased by connecting C67 in parallel with the switching diode GL13. In this range, AM is therefore only possible up to 5 kHz. A switchable RC section for suppression of the carrier (R70-R72-C69-C70) is connected between the detector and the control amplifier. It prevents the residual carrier which exists after peak detection from being fed back to the modulator, which would give rise to distortion of the RF signal.

The control amplifier feedback through a switchable RC section (R92-R93-C74-C76) determines the loop gain and ensures stability of the control loop.

The filter capacitor, carrier suppression and the loop gain are together switched over and controlled via the line "AM low" (ST1.6b). The control voltage passes from the output of the control amplifier B5 via T8 and ST1.13b to the modulator on board Y2.

The reference level for the control of the output level is fed in at ST1.2b via the amplifier B6. The diode GL18 compensates for the temperature characteristics of the detector diode. Potentiometer R101 permits adjustment of an offset which linearizes the slightly non-linear characteristic curve of the detector diode at low RF levels.

4.1.9 Modulation Control Y10

(See circuit diagram 302.7011 S)

4.1.9.1 Signal Flow

The signals for frequency modulation to drive the varicap diode (ST10.4b) and the reference level for the level control (ST10.11a) are produced on the modulation control board Y10.

The modulation signal is either produced in the internal modulation generator Y23, Y24 or is externally fed in to input 39 MOD. EXT. and passes to the modulation attenuator where it is attenuated by means of an attenuator with binary stepping so as to obtain the desired modulation depth or frequency deviation. The output signal of the modulation attenuator is available simultaneously at the level attenuator and deviation switch whose input switches are selected depending on the type of modulation (B80/IV for AM and B14/II for FM).
If AM is programmed as second modulation, external level control (ALC) or dual modulation is possible through socket 39 MOD. EXT. The two outputs of the ALC amplifier drive the level attenuator and the deviation switch. In FM or φM operation with AM as second modulation, the switch B80/III is switched on connecting the ALC amplifier to the level attenuator. The RF level can be varied by about 40 dB by means of a DC voltage of between 0 and 2.8 V applied to socket 39 MOD. EXT. In AM with FM or φM as second modulation, operation switch B14/III is in the "on" position and the ALC amplifier connected to the deviation switch. In this mode of operation, φM or FM is possible as second modulation in addition to AM through socket MOD. EXT.

4.1.9.2 Circuit Description of the Individual Subassemblies

The circuit section referred to as modulation generator in the circuit diagram is a Wien-Robinson-bridge oscillator (C1, C2, R1 to R6). The oscillator frequency can be switched over from 400 to 1000 Hz by means of the switching transistors T2-T3, which are driven from T1. In the SMFP2 only 1000 Hz is available. Frequency fine adjustment is effected by means of R1 (1000 Hz) and R2 (400 Hz). Gain control takes place in the feedback path of the oscillator amplifier B1/I by means of a FET (T4) which acts as a variable resistor whose resistance depends on the DC control voltage present at the gate. The DC control voltage is produced in a control amplifier (B1/II) by rectification (GL3-GL4) of the oscillator signal. The control voltage is adjusted such that the rectified oscillator signal is equal to the reference level present at the non-inverting input of the level amplifier. The diode GL2 compensates for the temperature characteristics of the rectifier diode GL3. The oscillator level is adjustable by means of R15. To minimize the distortion of the oscillator signal, feedback is applied to FET T4 via C3 and R21. Moreover, the oscillator drive can be set with R11 so that continuous oscillation is just maintained.

The output of this oscillator is taken via 19a to the socket <u>56</u> on the rear panel.
19b is used as input of the modulation attenuator. The binary-stepped attenuator consists of two parallel branches which are brought together in a summing amplifier (B7/II). In the one branch, the modulation values 0.5, 1, 2, 4 and 8% and kHz deviation, respectively, can be set and in the other branch, the values 16, 32 and 64. The summing amplifier is followed by a level attenuator (B8/I to II-B7/II) with switch-selected division ratios of 1:1 and 10:1.
If the modulation values are > 10, the division ratio 10:1 is selected and the 10-fold modulation value is set on the binary-stepped attenuator.
This permits setting of modulation values from 0 to 9.95 in steps of 0.05.

The level attenuator produces the reference level for the RF level control and the amplitude modulation. The DC voltage corresponding to the RF level is applied to the non-inverting input of the amplifier B9/I. Level switching between CW and AM is accomplished by means of the switches B80/I and B80/II.
The AC voltage corresponding to the modulation is applied to the negative input of B9/I via the switch B80/IV. A1C is possible via the switch B80/III.
As a result, a DC voltage, on which an AC voltage is superimposed in AM operation, develops at the output of the amplifier B9/I. This signal passes through a network of seven binary-stepped attenuator pads. Electronic switching permits

settings between 0 dB and 0.1, 0.2, 0.4, 0.8, 1.6, 3.2 or 6.4 dB. By appropriate combination, the RF output level can be attenuated by between 0 and 12.7 dB in steps of 0.1 dB. The actual transfer constant of each attenuator pad is 0.5% / dB less than its nominal value. This partly compensates the slight bend in the detector diode characteristic curve occuring at low levels. The RF output level is set by means of R76 (in CW operation) and R71 (in FM operation). For setting the modulation depth, R79 is used.

The deviation switch also contains an electronic switch at the input (B14/I and B14/II) which permits selection of the internal or external modulation source. φM or FM can be selected by connecting the link BR1 (plug-in type) accordingly. In the SMFP2, the link is always in the FM position.

In certain frequency ranges, the frequency-modulated RF signal passes through a 2:1 frequency divider and in other ranges (if fitted with the Option Frequency Range Extension) thorugh a doubler. In this way, the frequency deviation is either halved or doubled. To ensure, however, that the deviation of the output signal of the set is not affected by these internal operational states, the gain is switched over by the deviation switch. The gain of the stage B16/I is unity when the signal frequency is halved, 0.25 when it is doubled, and is otherwise 0.5. Furthermore, the RF signal passes through a mixer, the upper or the lower sideband being utilized depending on the frequency range. To make sure that the instantaneous frequency rises with the rising modulation voltage, the phase of the modulation voltage is shifted by 0° or 180° depending on the sideband. This takes place in the preamplifier B16/II which operates in the non-inverting mode (B15/I closed) or in the inverting mode (B15/III and B15/IV closed).

The control signals from the microprocessor are gated by means of a logic circuit such that the electronic switches are switched on or off depending on the selected operating modes. In CW operation, the switches at the input of the modulation attenuator (B3/I and B3/II) and of the level attenuator (B80/III and B80/IV) and at the output of the deviation switch (B15/II and B15/III) are open to give the minimum possible crosstalk between any modulation signal present and the AM and FM output.

The switches for the attenuator pads in the level and modulation attenuators are driven from a port expander (B25). The control signals from the microprocessor are sequentially received at the inputs 8 to 11 of this device and distributed to its outputs 1 to 5 and 13 to 23 where they are stored until new data arrive from the microprocessor.

4.1.10 Microprocessor Y11

(See circuit diagram 302.7111 S)

The circuit board Y11 carries the microprocessor which consists of integrated circuits of the MCS-48 family. B1 is a single chip microprocessor 8049 with 2K ROM program storage, B2 (8355) is a 2K ROM with two 8 bit I/0 ports. More ICs of the MCS-48 family are on other boards. There is one I/0 expander 8243 on each of the boards Y7, Y8 and Y10. The keyboard/display interface 8279 is on the keyboard/display unit.

The clock frequency for the 8049 is generated by an internal oscillator. The crystal Q1 is used as reference. Addressing of and data transfer to/from the ROM B2, the keyboard/display interface 8279 and the IEC bus is effected via the 8-bit bus DB0 to DB7.

To address the 2K program storage locations in B2, the bits 8 to 11 of the address are output by means of the port outputs P20 to P24.

For data output at the expander ports 8243 of the boards 8, 7, 10, addresses and data are output via the four port outputs P20 to P23 of the microprocessor 8049. The data transfer to/from the I/0 expanders 8243 is controlled by the signals $\overline{CS}$ 8243 8, 7, 10 (ST11 19a, 18a, 17a) and by the PROG. output of the µP 8049.

The signals I, J, K, L, M, N at the port outputs P10 to P15 of the µP 8049 have the following meaning:

Table 4-4

		High	Low
I	AM	On	Off
J	FM	On	Off
K	Modulation	Internal	External
L	Modulation	1000 Hz	400 Hz
M	Deviation, mod. depth	< 10 kHz, (%)	≥ 10 kHz, (%)
N		RF off	RF on

The binary-coded setting of the M divider is output at the port PA of B2. At port PB the BCD-coded setting of the attenuator is output.

By an INTERRUPT command, the µP 8049 is instructed to read in data via the bus. With remote control via the IEC bus, the INTERRUPT command is issued by the IEC-bus interface B17 on the microprocessor board. The INTERRUPT commands are combined at the input INT of the 9049 by the NAND gates B10 and B9/III-IV.

4.1.11 Attenuator Y45

(See circuit diagram 332.4010 S)

The attenuator is connected between the output stage and the output of the set. It permits the signal from the output stage to be attenuated by 140 dB in steps of 2 dB. Smaller level steps - as small as 0.1 dB - can be electronically achieved using the level control.

The attenuator comprises nine attenuator pads of 1 dB, 2 dB, 2 x 4 dB, 10 dB, 2 x 20 dB and 2 x 40 dB (R1 to R9) as well as ten through-line sections. The attenuator pads and through-line sections are of thin-film design. They are mounted on a total of 19 ceramic chips which in turn are soldered onto a base plate. Nine contact groups each with three switching contacts protrude between them through the base plate permitting switchover between attenuation and direct connection.

Each of these nine contact groups is operated by a rocker driven by a magnetic coil and held in its final position by means of a permanent magnet.

Transmission of the force from the rocker to the contact occurs by means of springs, which provide a uniform contact force of 20 gf. All contact surfaces are gold-plated.

The magnetic coils for attenuation switchover are driven from power gates (B1 to B5) which are linked via OR gates (B6) or via the control lines (drawn dashed) on the motherboard 2 such that BCD control is possible.
The 1-dB attenuator pad is used for switching off the output of the SMFP2 (after pressing the RF OFF key or upon triggering of the overload protection).
For this purpose, the last contact is omitted in the 1-dB attenuator pad.
In this way, the signal path is interrupted when switching on this attenuator pad.

The attenuator control values are shown in table 4-5.

Table 4-5

Attenuation	Attenuator pads switched on	Control lines on plug ST21 at "high" level
2	R7	2
4	R6	3
8	R1, R6	4, 11
10	R3	5
20	R4	6
40	R5	7
80	R2, R5	8, 15, 16
100	R2, R5, R8	8, 9, 13, 15, 16

4.1.12 1-GHz Frequency Extension SMFP-B2

Use of the 1-GHz Frequency Extension Option SMFP-B2 in conjunction with the SMFP2 extends the frequency range to 1000 MHz. The SMFP-B2 contains a doubler which produces the range 520 to 1000 MHz by doubling the frequency range 260 to 520 MHz.

The overall function is shown in the block diagram (Fig. 4-7). The signal derived from the output stage Y1 of the basic unit passes from the input of the SMFP-B2 either via the RF relay directly to the output (range up to 520 MHz) or via a diode switch to the doubler. On this PC board, there is an attenuator pad at the input for level adjustment. It is followed by the input filter which matches the impedance to the input resistance of the frequency doubler (approximately 25 Ω).

The frequency doubler consists of the four diodes GL 1I/II and GL 2I/II which operate as a full-wave rectifier. The two diode arms are driven in push-pull from the coaxial-line transformer TR1. To increase the doubler efficiency, the diodes are supplied with a quiescent DC current via the resistors R4 to R7 which can be balanced by means of R6 to minimize non-harmonic spurious frequencies.

The level attenuation introduced by impedance matching circuitry and the doubler is compensated for by the following amplifier B1 and the thin-film output amplifier. The doubled signal passes from the output amplifier via the detector and the diode switch at the output end to the RF output.
The detector forms part of the level control circuit. The rectified voltage obtained with the aid of the RF detector diode GL5 is applied to the non-inverting input of the control amplifier B2 where it is compared with the reference value supplied by the PC board Y10 and applied to the inverting input of the control amplifier via B3. The resulting control voltage adjusts the attenuation of the amplitude modulator on the PC board Y2 and consequently the RF level present at the input of the doubler such that the rectified voltage and the reference value are equal. Hence, this control circuit is designed such that a frequency- and load-independent EMF is obtained through the resistor R1 which acts as output impedance.

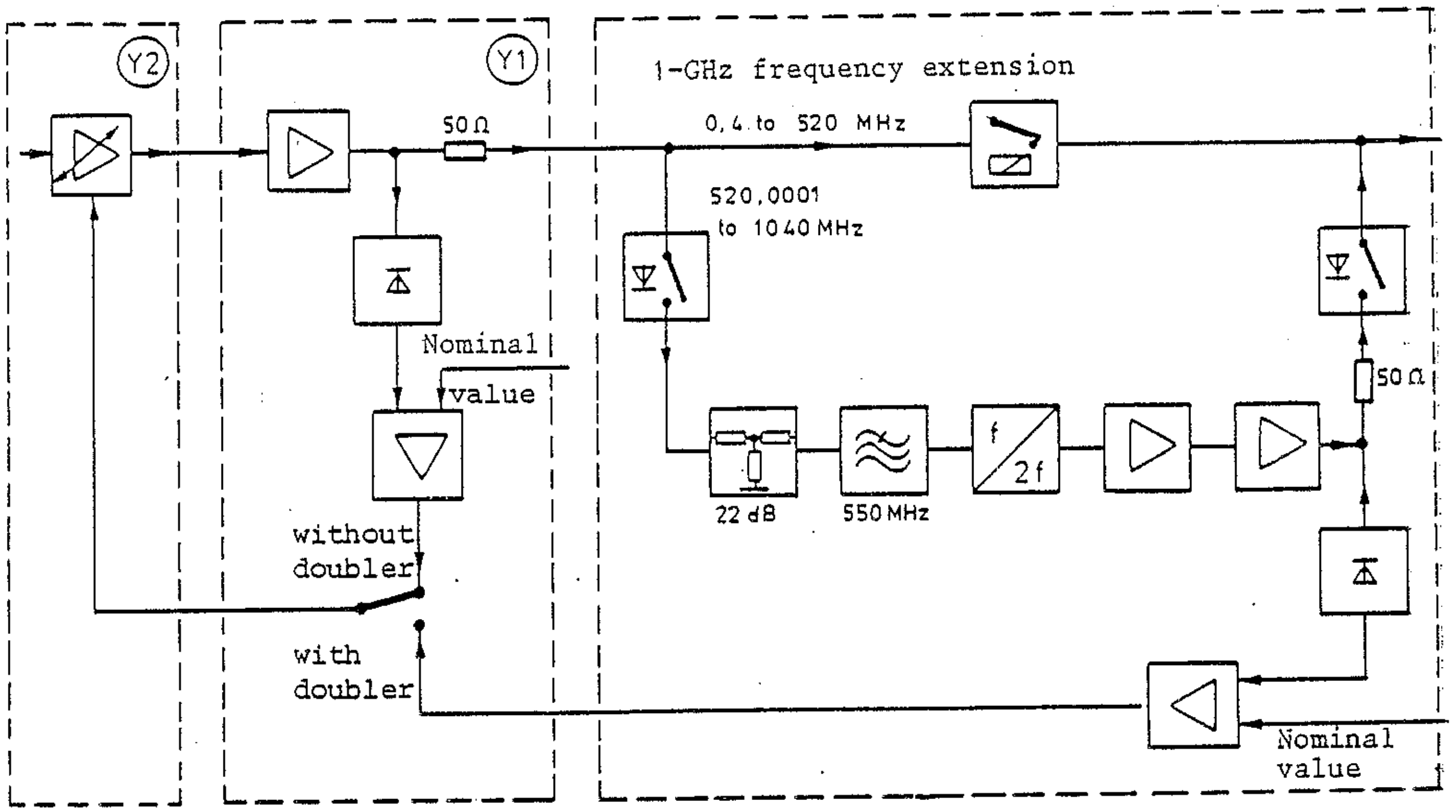


Fig. 4-7 Block diagram of 1-GHz Frequency Extension SMFP-B2

The RF output level is adjusted to the same value as produced by the reference value in the basic unit by means of the potentiometer R14.

The line from ST22.4 on the motherboard leads to the microprocessor on circuit board Y11 where its logic state is interrogated when the input frequency > 520 MHz. It is "high" if the SMFP-B2 is fitted. The computer will then accept input frequencies up to 1040 MHz. If the SMFP-B2 is not fitted, the line level is "low" and only input frequencies up to 520 MHz are accepted.

The microprocessor switches the RF signal path over via pin BU1.1 as a function of the frequency entered. This is accomplished by means of the relay RS1 and the diode switches B4 and B5, which are driven by the final stage T1-T2 and the switching amplifier B1. At frequencies above 520 MHz, the switching signal at BU1.1 is at "high" level.

4.1.13 Overload Protection Y46

The overload protection circuit protects the RF attenuator Y45 and the output stage Y1 against RF or DC voltages inadvertently applied to the RF output. To this end, the voltage present at the RF output is measured. If a threshold value is exceeded, a contact at the output of the RF attenuator switches connecting the 20-dB high-power attenuator pad of the RF distributor before the attenuator.

The RF voltage is fed out from the thin-film circuit B3 by means of a capacitive divider and after detection by a diode is taken from contact 2 via R2 to the comparator B1/II. An externally applied DC voltage is brought out at contact 1/B3. Positive voltages pass via R1 and GL1 directly to the comparator. Negative voltages are inverted in B1/I. The response level is set by means of R7. The switching signal for switching off the RF output passes from the comparator output via R11, GL5 and contact 4 to the RF attenuator. This signal is at "high" level if the overload protection is triggered. The integrated circuit B2 provides delayed resetting.

4.1.14 Reference Oscillator SMS-B1

The SMS-B1 is a plug-in unit. It is electrically connected to the reference board Y6 via four plug-in contacts A, B, C, D. For retrofitting the SMS-B1 remove the links BR1 and BR2 on the reference board Y6.

The crystal oscillator of the SMS-B1 consists of the crystal Q1, the oscillator transistor T16 and the resonant circuit TR1, C56, C57 and C58. C57 provides for temperature compensation of the transformer TR1 in the resonant circuit. C53 permits exact frequency setting. The transistor T13 acts as an emitter follower.

To keep the oscillator transistor and the crystal at a constant temperature, they are housed in an oven. The thermistor R60 is used as a temperature sensor and the transistor T15 as a heating element. The nominal temperature is determined by the factory-adjusted value of R52. The differential amplifier T10, T11 in conjunction with T12 forms the control amplifier. Current limiting of the heating transistor is accomplished via R58, GL10 and T12.

4.2 AF Synthesizer

The output frequencies of the AF Synthesizer are derived from the crystal-controlled reference frequency of the RF generator. In the digital section squarewave frequency is produced by programmed frequency division of a 100-MHz oscillator. This squarewave frequency is applied to the sinewave shaper where the sinusoidal shape and the correct output signal level are produced.

4.2.1 Digital Section Y24

(See circuit diagram 356.5717 S)

A 100-MHz signal synchronized with the crystal-controlled reference frequency of the RF synthesizer is produced in B30, B32, B37, B10 using a PLL.

This is followed by a programmable divider which operates at the same time according to the fractional division method and the pulse swallow method. B12, a high-speed ECL prescaler with a division ratio of 10:1 and 11:1 is controlled from the auxiliary divider B60, B61. The signal of about 10 MHz available at the output of B12 is applied to a monoflop where it is expanded and subsequently split up between the following two paths:

1) to the programmable synchronous divider B20 to B23 at whose output the AF clock pulse for the sinewave shaper is available;

2) to the auxiliary divider B60, B61.

The auxiliary divider which is a shift register outputs the data applied in parallel to its input in serial to the prescaler at a rate of 10 MHz once during each AF clock pulse thus determining the division ratio 10:1 or 11:1.

The process described above is the well-known pulse swallow frequency division method.

B62, B63 and B64 are used for the fractional division method.

B62 to B64 is an up-counter with programmable step size which produces an overflow signal at the figure 256. The counting rate is the output signal of the synchronous divider B20 to B23. The step size is supplied from the store modules B72, B73 to an input of the adder B63, B64. If an overflow occurs (pin 9, B64) an additional "1" is input into the shift register which acts as an auxiliary divider, causing the 1:10 division cycle at B12 to be replaced by a 1:11 cycle at longer intervals. The additional 100-MHz period thus used up increases the division ratio N by an amount < 1 (fractional division). Example: N = 200.1 is produced by 9 times dividing by 200 and once by 201.

The data are transferred in the following manner: The eight shift registers (serial in - parallel out) in B50 to 53 which are used as buffers for storage of the four 8-bit data words output these data as a 32-bit data word to the store modules for the synchronous divider, auxiliary divider and fractional divider B40 to B43 and B70 to B73. Transfer to the latter store modules is accomplished with a single transfer clock pulse ensuring immediate setting of the new frequency.

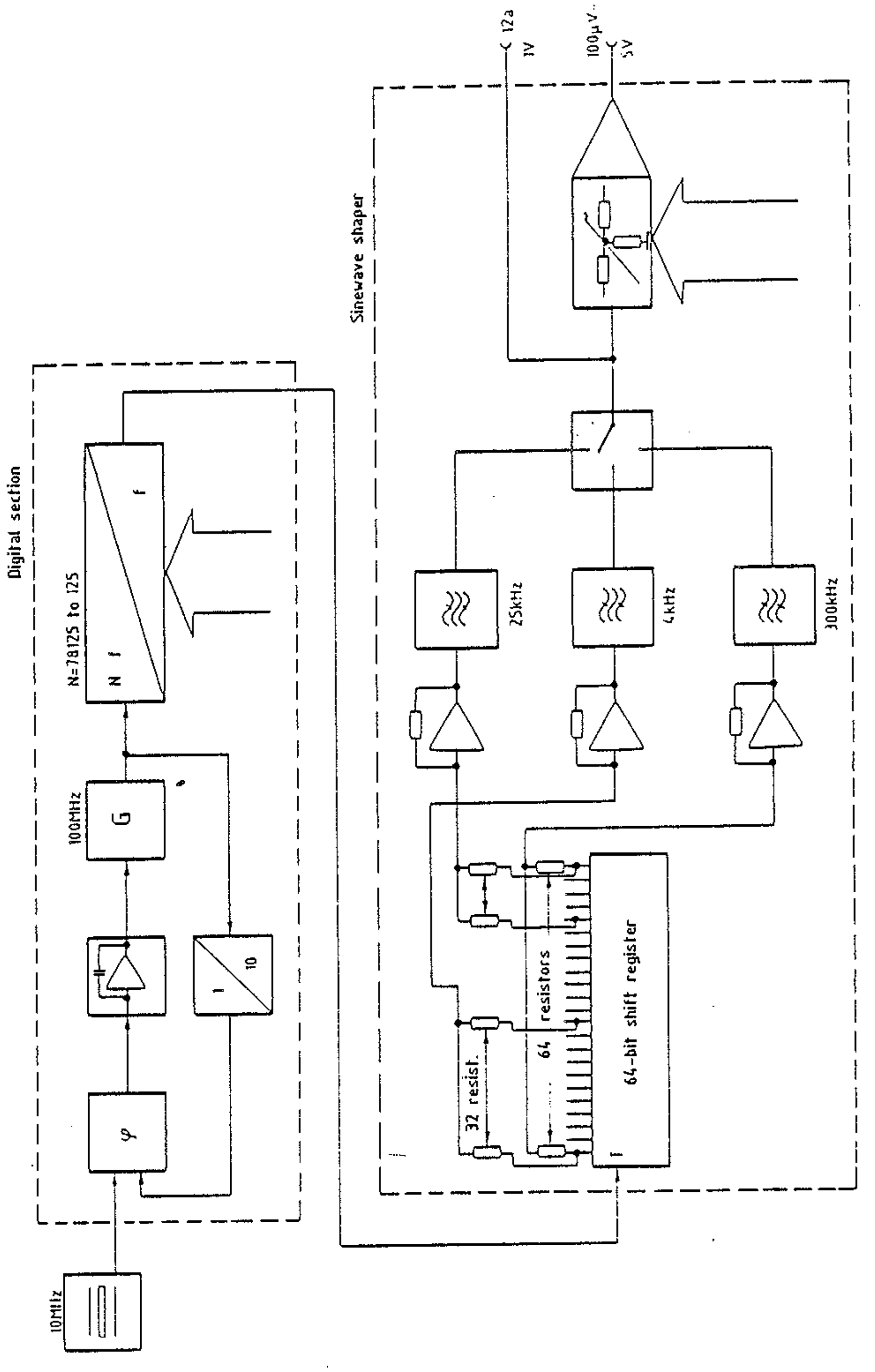


Fig. 4-8 Block diagram of AF Synthesizer Option SMFS2B7

4.2.2 Sinewave Shaper Y23

(See circuit diagram 356.5517 S)

The AF clock pulse supplied from the digital section to the sinewave shaper is converted into a sinewave voltage as follows. First, a vacant 64-bit CMOS shift register (serial in - parallel out) is loaded with ones via the serial data input at the AF clock pulse rate. A resistor is connected to each parallel output. The other end of these resistors is connected to the summing junction of a summing amplifier. The resistance values are chosen such that when loading the shift register a sinusoidal staircase voltage is obtained at the output of the summing amplifier (half-wave from the trough to the peak). After loading the shift register with ones, it is loaded with zeros. As a result, the falling half-wave of the sinusoidal staircase voltage is obtained at the output of the summing amplifier.

The 64-bit shift register B4 to B11 is used for the frequencies 10 Hz to 300 Hz. The logic level present at the serial data input of the shift register is obtained by frequency division (1:28) of the AF clock pulse in B3.

A 32-bit shift register must be used for the frequencies 300 Hz to 4 kHz and a 16-bit shift register for the frequencies 4 kHz to 25 kHz. The parallel outputs of the same shift registers are used as for the lower frequency range but only part of the 64 outputs. Frequency division of the AF clock pulse for producing the correct data at the serial data input of the shift register takes place in B3, but other outputs are used.

A 6th order low-pass filter is connected into the signal path for each frequency range (B12 for 300 Hz, B13 for 4 kHz, B11 for 25 kHz).

The CMOS gates B1 and B2 for selection of the data clock and the analog switches B16 and B17 for selection of a frequency range are controlled from the common lines a12 and a13.

The second task of the sinewave shaper is to produce the output level. B19, B23 act as a programmable 10-bit voltage divider. The voltages 0 to 2.5575 V can be programmed at MP5 in steps of 2.5 mV. Subsequently, the voltage is boosted by a factor of 2 or 0.4. The relays connect the output signal either directly or via a fixed voltage divider to the output.

The programmable voltage divider, the switch-selected gain and the fixed voltage divider permit the following output voltages to be obtained:

0	to	100 mV	in steps of	100 µV
100 mV	to	1 V	in steps of	1 mV and
1	to	5 V	in steps of	5 mV.

The output impedance is < 2 Ω. The minimum output current load required is 50 Ω. The output is shortcircuit-proof.

The CMOS store modules B20 to B22 act as the data input expander to transmit the 10 data bits from the 8-bit data bus in parallel to the programmable voltage divider and at the same time drive the relay and the switchable voltage amplifier.

4.3 Measuring Section

4.3.1 RF Distributor Y47

(See circuit diagram 332.0015 S page 4)

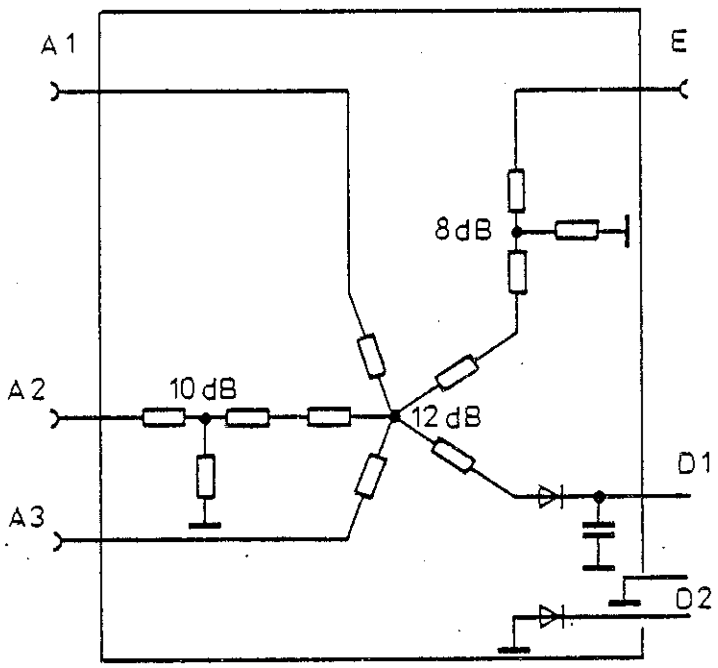


Fig. 4-9 Functional diagram of RF distributor Y47

Terminal E of RF distributor Y47 is connected to the RF input/output socket 48 on the front panel via a switch.

Terminal A1 is connected to the other switchable attenuator pads of the RF attenuator via a switch. If the RF signal supplied by the RF generator section passes from A1 to E (receiver measurement mode), the RF distributor serves merely as a 20-dB attenuator pad (equivalent to the other switchable attenuator pads of the RF attenuator).

If an RF signal is applied to E (transmitter measurement mode), it is attenuated by 30 dB and taken to A2 from where it is fed to socket 54 on the rear panel. At the same time it is taken to A3 after it has been attenuated by 20 dB. From A3 it is taken to the input of the RF amplifier.

On a third path it is taken - again after attenuation by 20 dB - to a peak-value rectifier, the output signal of which is applied to the DC amplifier board for measurement of power and for AM measurement. The fourth possible path from E to A1 is meaningless in the transmitter measurement mode. The 8-dB attenuator pad is a high-power attenuator pad since transmitter powers up to 30 W are permitted at terminal E.

4.3.2 RF Amplifier Y31

(See circuit diagram 332.1570 S)

The RF signal applied to the RF power input and attenuated by 30 dB in the RF distributor, or that applied to the SMFP2 frequency meter input, is amplified by an RF amplifier with automatic gain control. The output signal passes directly to the mixer board Y32 and via an additional amplifier to the counter Y33.

The inputs ST312 (frequency meter input) and ST311 (RF distributor) are switched by means of the diode switches GL24, B3 and B1, B2. The additional diode GL23 in conjunction with R98 provides matched termination of the RF distributor when using the frequency meter input. Switching is accomplished via b7 and the voltage comparators B6I to B6IV. From the diode switch, the RF signal is taken via the PIN diode attenuator GL6 to GL10 to the actual RF amplifier T8 to T11, the output level of which is measured by means of GL12I, compared with a reference value adjustable by means of R57, and controlled via the integrator B4I and the PIN diode attenuator. Hence, the comparator B4II gives an indication to the computing controller Y21 via a6 if the control range is exceeded in the case of insufficient input voltages (TTL "high"). The time constant of the integrator B4I is fixed by means of C32 such that an amplitude modulation of the RF signal is partly levelled out providing sufficient voltage for the frequency counter even for dips in the modulation envelope. If the output signal of the RF amplifier is taken to the adjacent-channel power meter via the mixer, the control circuit incorporating T13 is interrupted and the control voltage (from the adjacent-channel power meter) is taken from b4 via T12 to the PIN diode attenuator. Switching of the control circuit is effected via b10 and the voltage comparators B5III and B5IV.

The output signal of the RF amplifier is taken via ST313 directly to the mixer board Y32, on the one hand, and via the 6-dB thin-film amplifier B8 and ST314 to the counter Y33, on the other.

In addition, the output voltage of the RF amplifier is taken via a high-pass filter and a low-pass filter to the diodes GL20II and GL20I where its level is determined. The cut-off frequency and rate of cut-off of the two filters are dimensioned such that the test voltages of GL20I and GL20II are about equal (fine adjustment by means of R87) at a frequency of approximately 530 MHz. The voltage comparator B7 connected in series converts the RF level differences between the two test points for frequencies < or > 530 MHz to TTL level and indicates to the computing controller Y21 when the frequency of the RF amplifier input signal is above or below 530 MHz. The computing controller, in turn, switches in a 4:1 RF prescaler in the counter if the frequency is > 530 MHz.

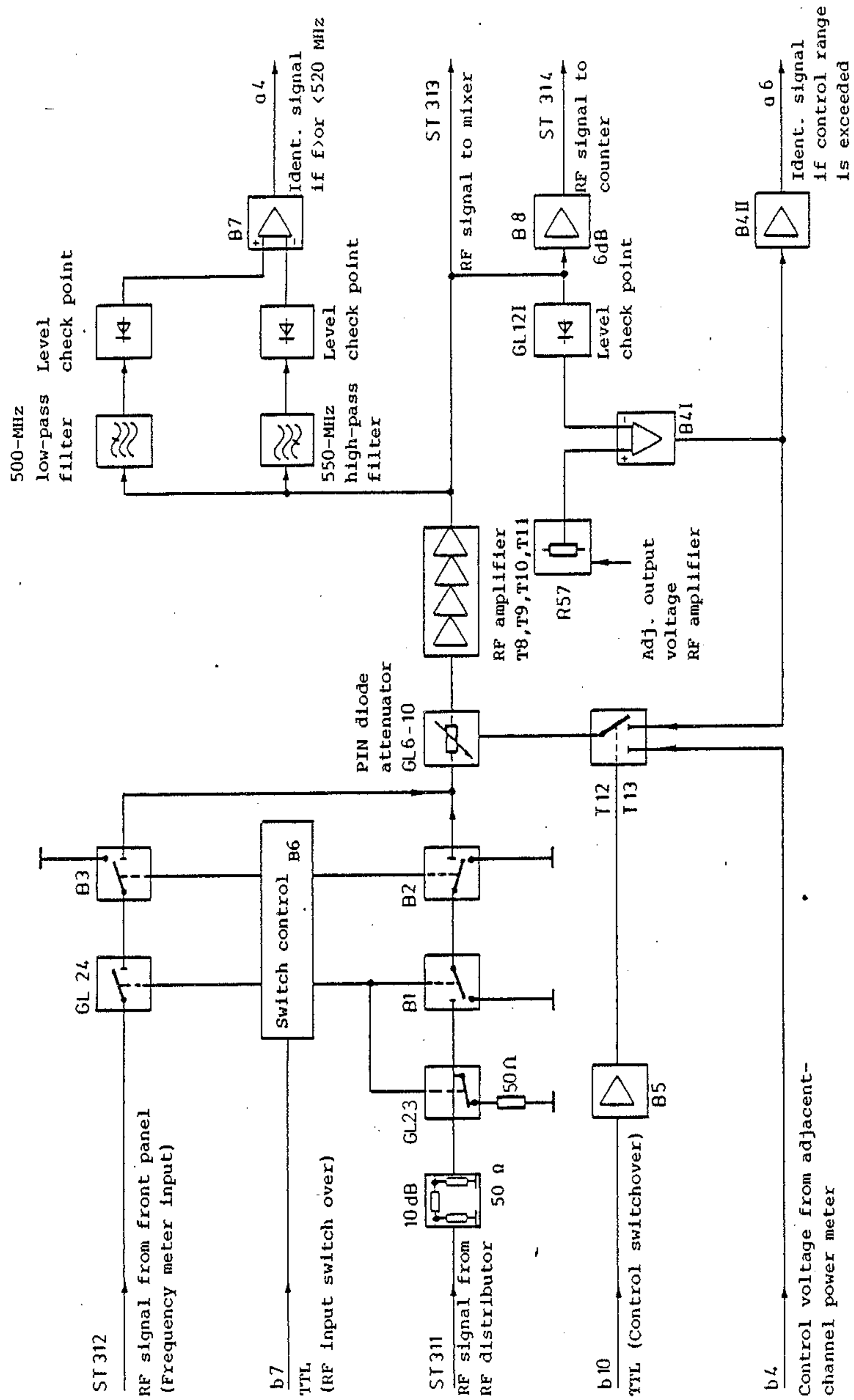


Fig. 4-10 Block diagram of the RF amplifier

4.3.3 Mixer Y32

(See circuit diagram 332.1611 S)

The output signal of the RF amplifier (signal to be measured applied to the RF power or frequency meter input) is mixed with the signal of the internal RF generator to produce the intermediate frequencies for the FM and the φM demodulator (200 kHz) and the optional adjacent-channel power meter (455 kHz ± n · channel spacing). In addition, the difference frequency between the frequency of the input signal (front panel) and a frequency of the internal RF generator selected via the keyboard of the SMFP2 is obtained in the mixer for beat-frequency measurements.

The flow diagram below gives a general picture of the control and the coordination of the frequency counter Y33, mixer Y32 and RF generator modules.

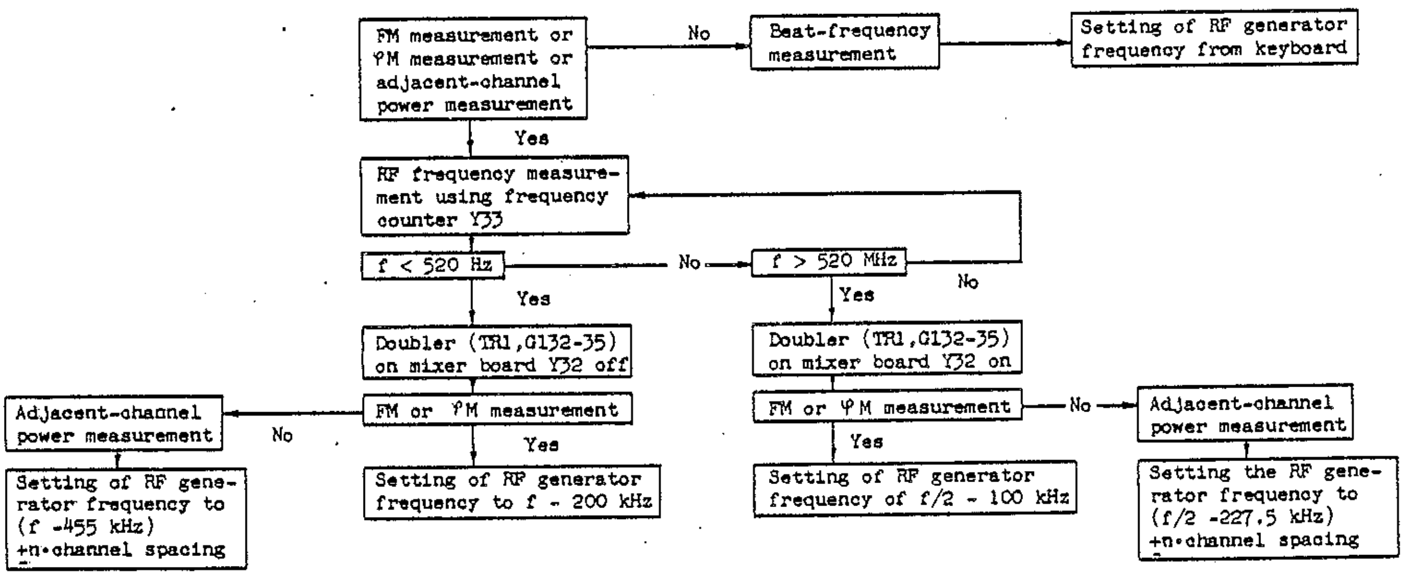


Fig. 4-11 Flow diagram for the control of the Y33, Y32 and the RF generator modules

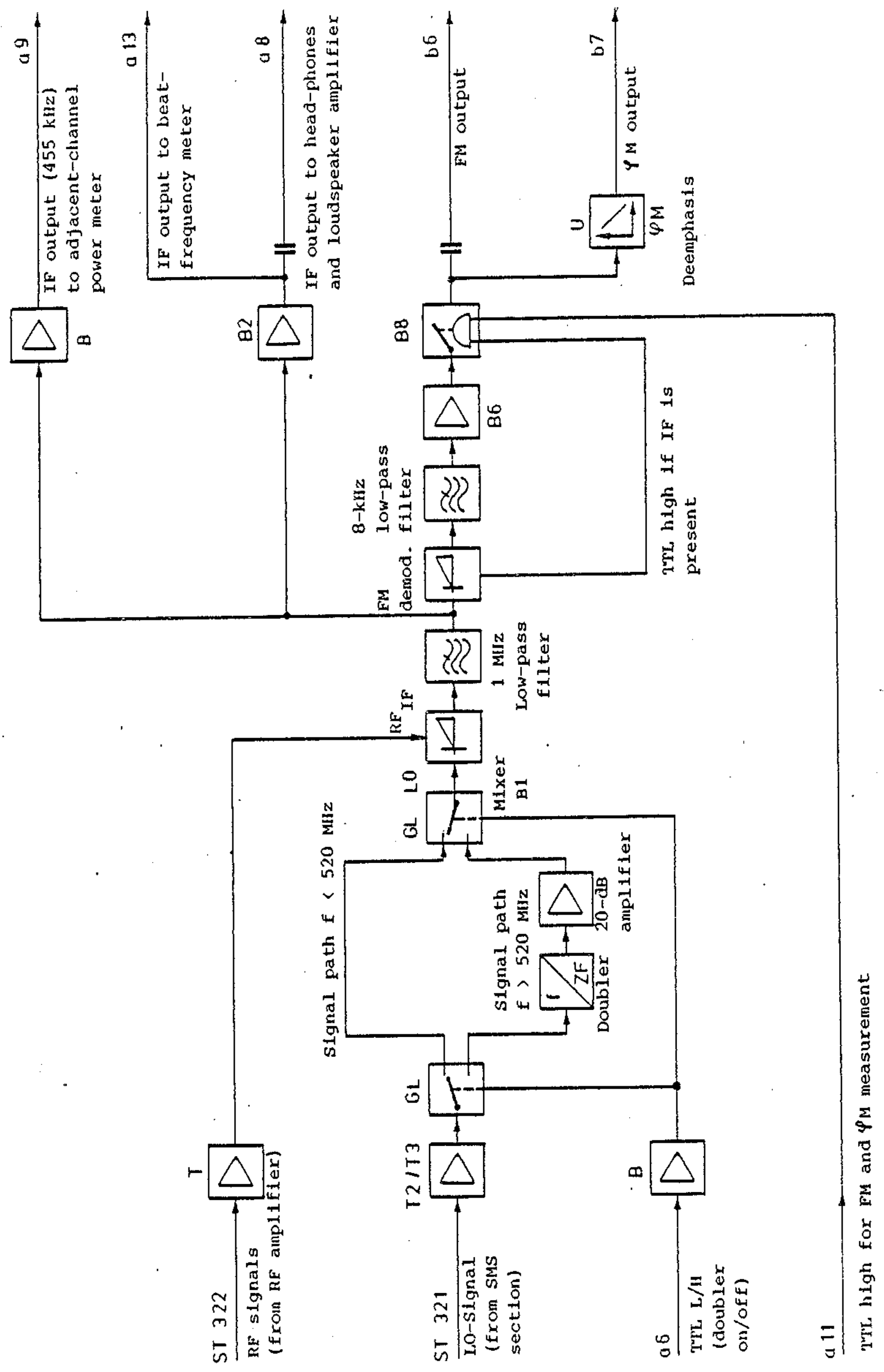


Fig. 4-12 Basic diagram of the mixer

The test signal arriving from the RF amplifier Y31 via ST322 is taken via amplifier T1 and attenuator R9-R11 to the mixer B1. The local oscillator signal is taken from the RF generator of the SMFP2 via ST321 to the amplifier T2 and T3 where it is boosted and subsequently applied directly via K1 if f < 520 MHz or, if f > 520 MHz, via the doubler TR1, GL32-35 and the cascaded amplifier B30 to the mixer B1. The two paths for the local oscillator signal are switched under computer control via a6, comparator B40 and the diode switches GL30/31 and GL36/37. The RF signal is then together with the local oscillator signal converted into the required IF (FM and φM: 200 kHz; adjacent-channel power measurement: 455 kHz ± n · channel spacing; beat-frequency measurement: difference frequency between RF signal and RF generator frequency entered via the keyboard).

The output signal of the mixer B1 (IF) is taken via an IF filter (local oscillator signal and RF filtered out, 50 Ω matching at all frequencies) to the various signal paths:

Measurement	Signal path	Output	Module connected
Adjacent-channel power measurement	B80	a9	Adjacent-channel Power Meter SMFP-B6
Beat-frequency measurement (frequency measurement)	B2	a13	AF amplifier Y35
Beat-frequency measurement (Headphones, loudspeaker)	B2	a8	Regulator Y38
FM measurement	B4, B5, T9/10, B6, B8	b6	AF amplifier Y35
φM measurement	B4, B5, T9/10, B6, B3II, B3I	b7	AF amplifier Y35

For FM and φM measurements, the mixer output signal is converted to TTL level by means of the comparator B4 and taken to the monostable B5 where square-wave pulses of constant pulse duration and a duty cycle dependent on the frequency deviation are produced. The two output signals of the monostable B5 (Q and $\overline{Q}$) are brought together via the difference amplifier T9/T10 to enhance demodulator efficiency and are fed via an 8-kHz low-pass filter (L32/33, C69/61/71) which filters out the 200-kHz IF to the output amplifier B6 of the FM demodulator.

Through the electronic switch B8, the demodulated signal is fed via the coupling capacitor C74/75 to the FM output b6 and via the deemphasis filter B3II/I to the φM output b7. The logic input function of switch B8 enables the signal path only if the information for an FM or a φM measurement (TTL "high") is present, and at the same time the presence of an IF signal is indicated (TTL "high") by means of the retriggerable monostable B7 which is driven from an auxiliary output of B5 (pin 1). This prevents the coupling capacitor C74/75 from becoming charged when the demodulator is inoperative and reduces the settling period time constant of the deviation meter to a minimum.

To ensure minimum inherent spurious deviation of the deviation meter, all individual circuits of the demodulator susceptible to voltage fluctuations are supplied via the additional voltage regulators (B50II/T15, B50I/T16, B51/T17).

4.3.4 Counter Y33

(See circuit diagram 322.2118 S)

Three different signals are delivered to the counter board where their frequencies are counted.

1. RF signals with frequencies between 1 MHz and 999.99999 MHz:
   These are fed from the front panel via the RF amplifier board where their level is kept constant at 150 mV_{rms} (ECL) to the prescaler or the RF stages on the counter board Y33.

2. AF signals with frequencies between 10 Hz and 1 MHz:
   These are fed from the front panel to the AF amplifier board where they are converted to TTL level and from there via gates to the AF counter stages on the counter board Y33.

3. Demodulated signals or beat frequencies in the AF range:
   These are also fed from the AF amplifier with TTL level via gates to the AF counter stages on the counter board Y33.

The frequency counting for all three signal paths is effected in the following manner:

After all BCD outputs of the 8 cascaded 10:1 counter stages have been reset via the Reset line (a12), the microprocessor produces a count gate of exactly 1 s, 0.1 s or 0.4 s.

At the end of this gate time, the figures present at the BCD outputs are transferred in "8-bit parallel" and "serial byte" format to the data bus. After they have been checked by the microprocessor, they can be displayed without conversion.

A frequency discriminator on the RF amplifier board supplies the signal RF > or < 520 MHz to the microprocessor. If the signal is RF > 520 MHz, the microprocessor produces a gate time of 0.4 s and resets all which causes the RF to be fed via the 1:4 prescaler B23, via the RF switch B20 and the limiting amplifier T1 to the RF counter stage B5. If the signal is RF < 520 MHz, the RF is taken directly to the limiting amplifier via the RF switch B21 whilst the 1:3 prescaler is switched off by cutting off the supply voltage.
In this case, the gate time is 0.1 s. In either case, the gate time is produced with the aid of a clock inhibit signal which is fed to the first counter stage B5. The NAND gates in B1 are switched such that the signal to be counted between B6 and B7 is connected through. If AF or beat frequency is to be counted, the signal to be counted is fed from the pins b12 or b13 via the gates in B1 to the counter stage B7. The RF counter stages B5 and B6 are now inoperative. In this case, the gate time (1 s) is produced by switching the decoder B22 as appropriate with the aid of the microprocessor.

For counter readout, the microprocessor successively triggers the pins b8 to b11 which causes two of the eight bus driver ICs B11 to B18 at a time to transfer the TTL levels present at the inputs 2, 5, 9 and 12 via the data bus to the microprocessor.

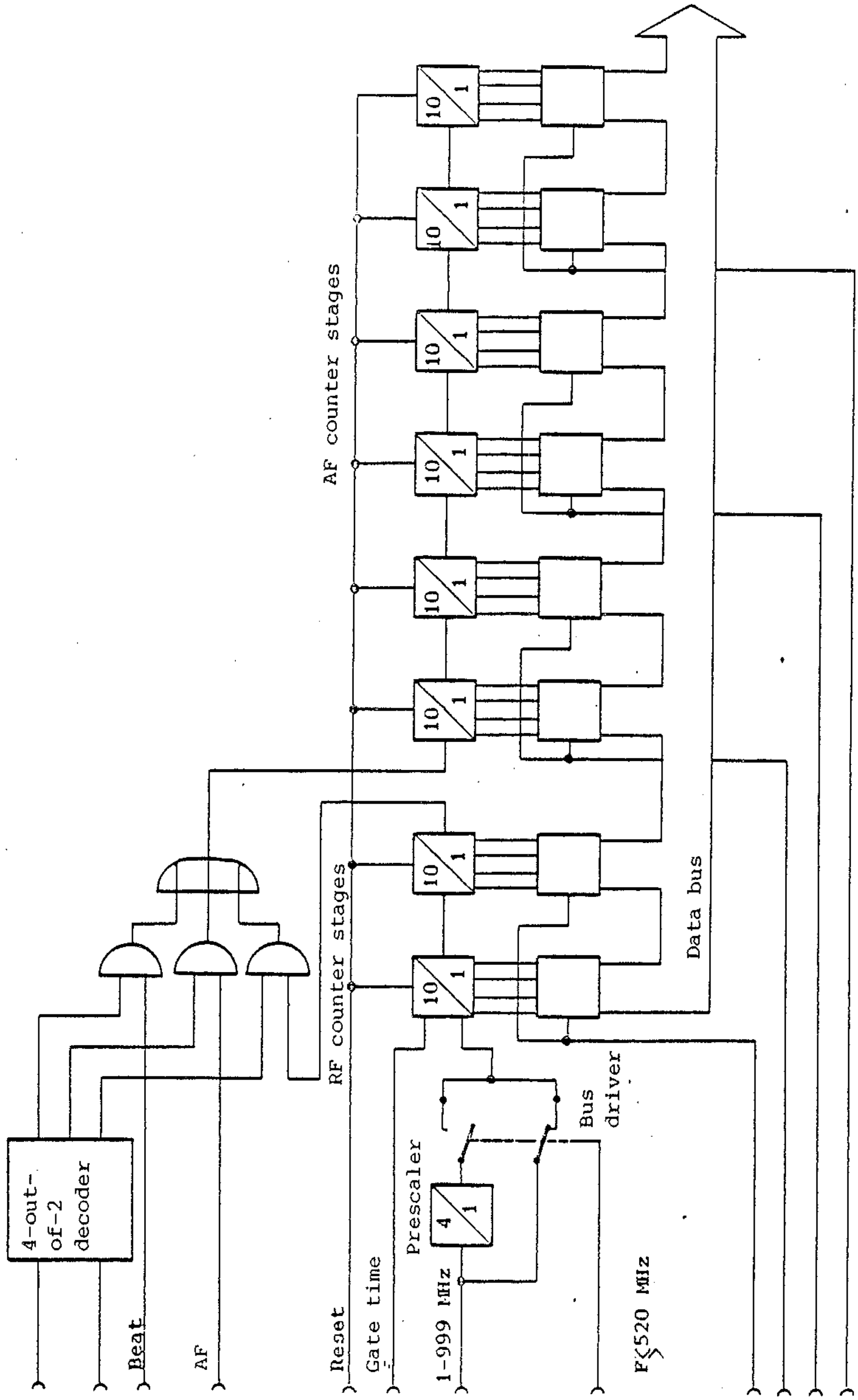


Fig. 4-13 Block diagram of counter

4.3.5 AF Amplifier Y35

(See circuit diagram 332.2618 S)

All AF signals in the SMFP2 whose level or frequency is to be measured are taken to the AF amplifier where they are matched to the dynamic range of the detectors in the next stage (DC amplifier Y37) and the counter input stages (counter Y33) by means of switchable amplifiers and signal limiters.

Depending on the measurement to be carried out, the input signal is taken via one of the FET switches T22-T25 and B19 from the input 5b (AF external), 6b (FM measurement), 8b (φM measurement) or 11b (AM measurement) via output 17b to the filter board Y36 (through-line section, harmonic filter or CCITT filter) and via input 19a back to the AF amplifier where it is amplified by 0, 20, 40 or 60 dB, depending on the level, with B30, B35 and B40. The gain is adjusted by means of the computing controller Y21 via 9a, 10a, 11a and the FET switches T30, T35, T40. The level determined in the preceding test cycle by means of the detectors (on DC amplifier Y37) and the A/D converter (Y22) serves as criterion for the adjustment (gain increase or decrease by 20 dB if the level falls below the range or exceeds the range). From test point 3, the signal is taken via the 20-kHz low-pass filter, buffer amplifier B50 and output 18b to the rms- and peak-value detector on the DC amplifier Y37. Moreover, the signal is fed via B55 and 9b to the socket 37 DEMOD. SIGN. on the front panel of the SMFP2.

For frequency measurement, the demodulated FM, φM or AM signal is delivered to the counter Y33 via buffer amplifier B45, switching transistor T61 and the limiting amplifier T65/T70 through output 13b. For beat-frequency measurement, the signal path is interrupted by means of T61, and the difference frequency from the mixer Y32 via input 13a is fed into circuit via T60.

For external frequency measurement, a signal is applied to socket 31 on the front panel of the SMFP2 and passes via input 5b and the buffer amplifier B18 to the limiter GL1/2 of the counter control and from there on to the emitter follower T1, amplifier B5 and the comparator B10 (TTL). Via output b12, the signal is taken to the counter Y33. The operational amplifiers B15I and B15II supply the voltage for the counter control.

4.3.6 DC Amplifier Y37

(See circuit diagram 332.2830 S)

The DC amplifier board contains several functional units:

The AF signals from the AF amplifier with voltage levels of as a rule between 3.54 V_{rms} and 0.354 V_{rms} are rectified here. Detectors for this purpose are present in the rms-reading and the peak-reading meter. An inverting amplifier with a gain of unity is connected to the input of the peak-reading meter so that positive and negative peak values can be measured.

For the rms-reading meter, the IC AD 536 A is used which supplies a DC output voltage corresponding to the true rms value of an input signal of any shape.

The integration time constant required for the generation of the rms value is 200 ms so that frequencies down to about 50 Hz can be rectified by the rms-value detector. An output voltage of 10 V DC at test point 1 (B15) corresponds to a voltage of about 3.54 V_{rms} at the input of the board.

The peak-reading meter consists of the operational amplifiers B11 and B12. The peak value measured is held about 0.15 s which permits voltages with frequencies down to 10 Hz to be rectified by a peak-value detector. An output voltage of 10 V at test point 6 (B12) corresponds to a voltage of 5 V_s at the input of the board.

A further functional block is formed by the impedance converters for the test parameters applied to the sockets 28 during voltage and current measurement and for the test voltage from the RF detector.

The difference amplifiers B1 and B2 with a gain of unity are used when measuring current. The inputs a5, a6 and a17, a18 can be driven with common-mode input voltage of +30 V.

The difference amplifier B3 is used when measuring voltage. It has a gain of 1/2. Voltages up to +30 V referred to ground can be applied to inputs 7a and 8a. The impedance converter is preceded by relays which ensure that the capacitor C40 is charged prior to the measurement until it is equal to the voltage between a5 and a6. Even if a high common-mode input at B1 causes an error due to inadequate common-mode rejection this error is avoided by opening the relay contacts prior to the measurement proper and applying the voltage at C40 without common-mode input at the time of the measurement via B1 to the D/A converter for further processing.

A similar circuit is provided in the current measurement range II (B2).

The measured voltage from the RF rectifier is available between a9 and a10. The diodes in the RF rectifier are normally biassed via R27 and R28 against -15 V in the forward direction.

But if a positive voltage is applied to the diodes in the RF rectifier from B80 and T80 via R27 and R28, they are cut off to prevent them from causing distortion in the RF branch.

Power can, however, be measured via the differential amplifier B4 only if the diodes in the RF rectifier are biassed in the forward direction. The difference voltage between a9 and a10 may either be a DC voltage or a DC voltage with a superimposed AC voltage.

The DC component, which is produced at R34 and C6, or one of the output voltages from B1, B2 or B3 is taken to the DC output b11 via FET switches.

At the same time, the DC voltage with superimposed AC voltage is taken to a controlled amplifier B6, B8 at the output of which (MP4) the average value of the DC voltage is kept constant to 5 V. C10 decouples the DC voltage and the AC voltage is taken to the AM output b8 for measurement of the modulation depth.

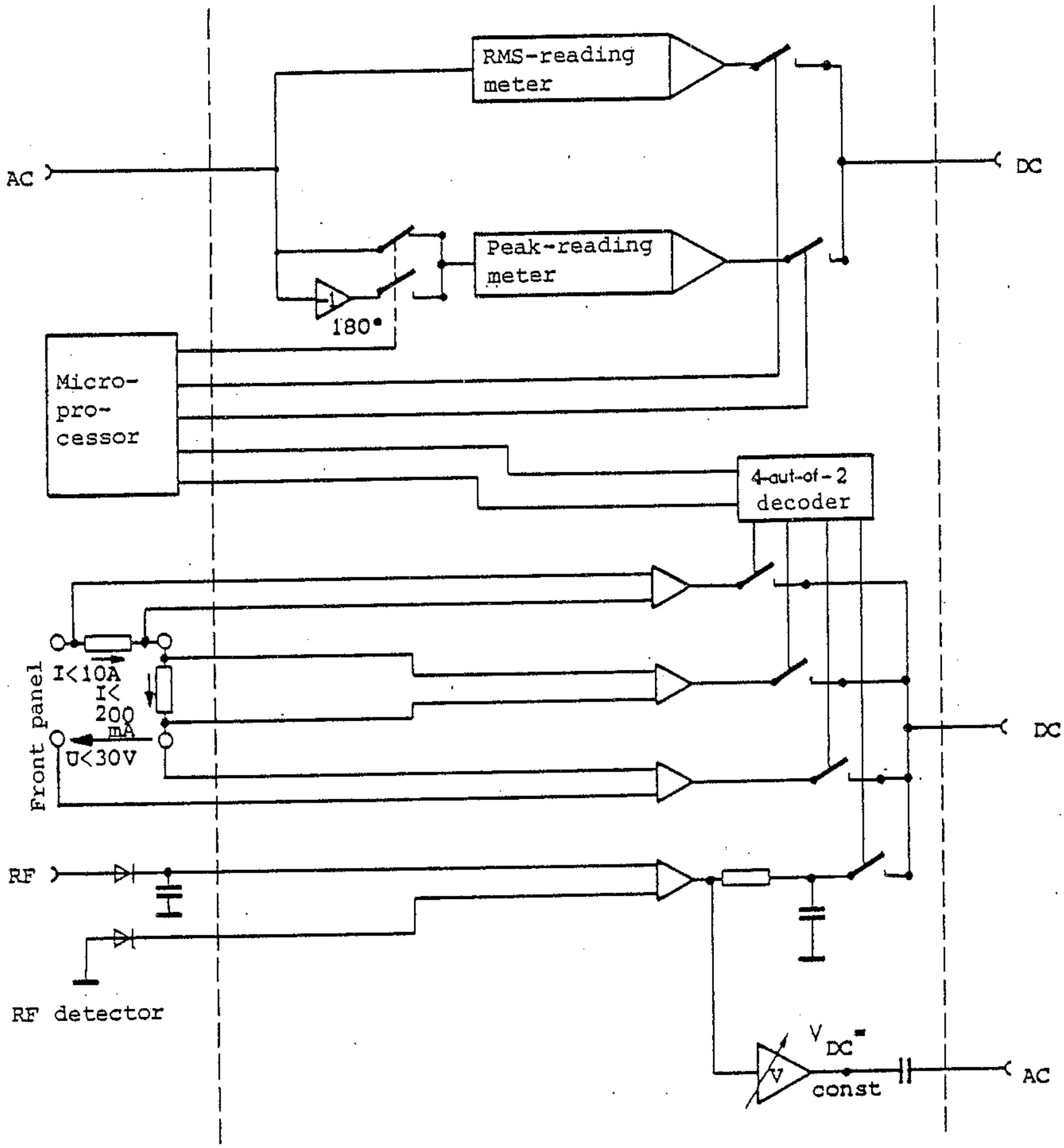


Fig. 4-14 Basic diagram of the DC amplifier

4.3.7 A/D Converter Y22

(See circuit diagram 355.2814 S)

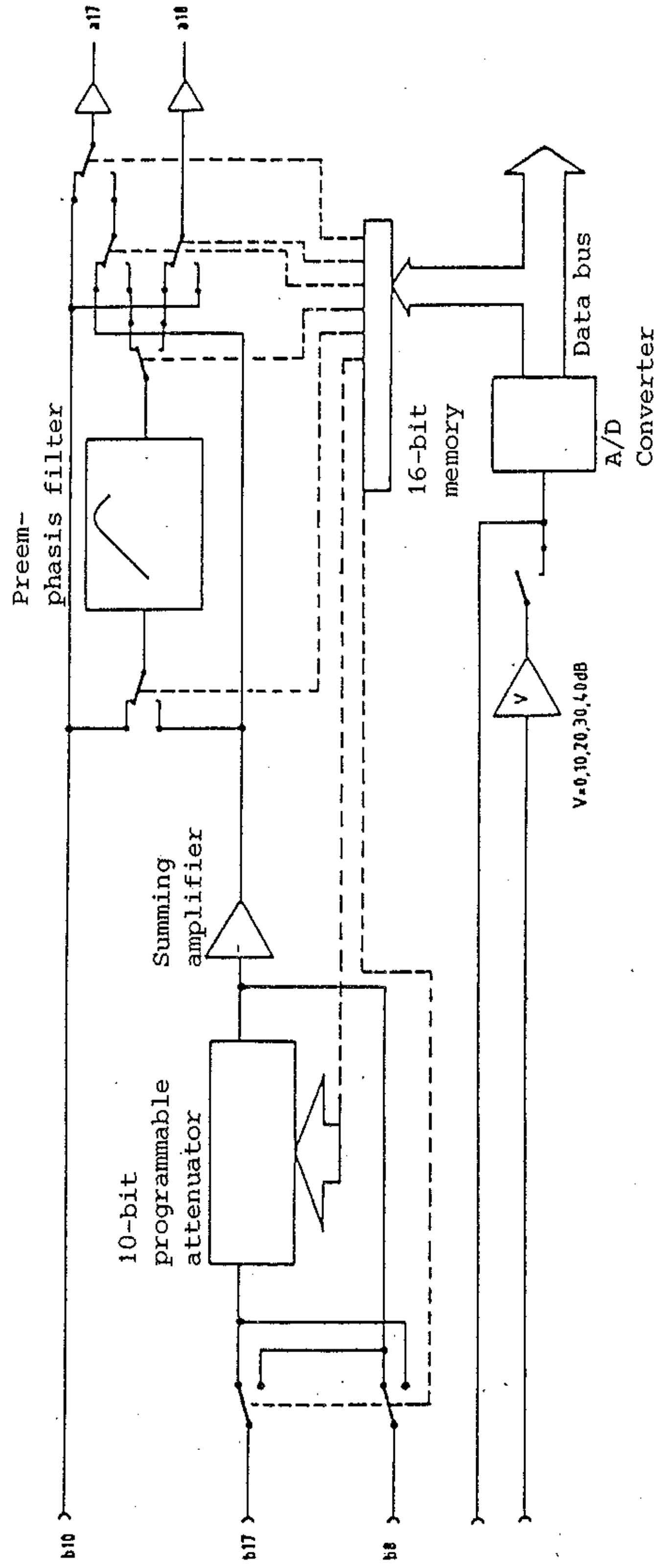


Fig. 4-15 Basic diagram of the A/D converter

The A/D converter board carries two independent functional sections:

1) The modulation processing section including the preemphasis filter with various switches and a programmable attenuator.

2) The 10-bit A/D converter with a DC amplifier with switchable gain.

The modulation processing section has three inputs:

b8 from the AF synthesizer

b17 from the 1-kHz or the 400-Hz RC generator Y10

b19 from the front-panel socket 39 MOD. EXT.

and two outputs:

a17 to modulation input with modulation attenuator and

a18 to modulation input without modulation attenuator.

Either of the two input signals from b17 or b8 can be applied directly or through the programmable attenuator B3/B4 to the summing amplifier B5 through either switch B1 or B13. The two signals are added in B5. This device permits modulation of the SMFP2 with a doubletone and the modulation depth or frequency deviation of the two tones can be programmed independently thanks to the attenuator B3/B4 which is programmable with a resolution of 10 bits.

By switching in the following preemphasis filter, a φM modulated signal can be obtained from the RF generator, which normally supplies only FM modulated signals. The switches preceding and following the preemphasis filter, in conjunction with the AM and FM RF generator section, permit single and dual modulation:

The 10-bit A/D converter B24 operates synchronous to the computer as follows:

The A/D converter causes the "Data valid" line (a10) to go "high" if valid data are present at the digital outputs 3 (MSB) to 12 (LSB) from earlier A/D cycles. During A/D conversion, the "Busy" line (a9) goes "high".

The computer initiates A/D conversion with a short positive-going pulse on the "Initiate conversion" line (a8) and reads out the result from the tri-state drivers B25, B26 and B27 in two sections via the data bus after interrogating the "Busy" and the "Data valid" lines.

The A/D converter handles positive DC input voltages between 0 and 10.23 V. One digit corresponds to 10 mV. A DC amplifier with switchable gain (0, 10, 20, 30, 40 dB gain) is connected to the input of the A/D converter to enable it to operate in its upper dynamic range (1000 to 10023 mV) even with small DC input voltages.

The gain is switched by switching the resistors R35, R42 and R43 either into or out of circuit by means of the FET switches T1, T2 and T3.

4.3.8 Filter Y36

(See circuit diagrams 332.2799 S and 332.2899 S)

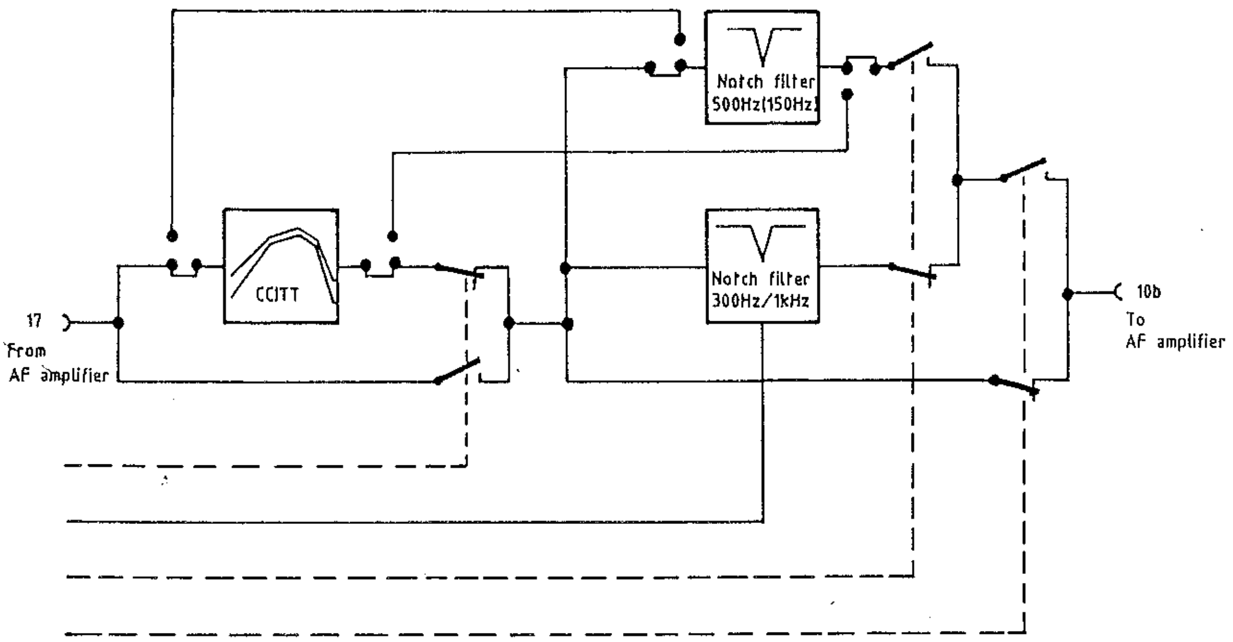


Fig. 4-16 Block diagram of filter

Table 4-6 Filter control

		1:CCITT 0:Through-connection	1:300 Hz 0:1 kHz	
8a	7ab	6ab	5ab	
X	0	0	X	Through-connection
0	1	0	X	500-Hz notch
1	1	0	0	300-Hz notch
1	1	0	1	1-kHz notch
X	0	1	X	CCITT
0	1	1	X	CCITT with 500-Hz notch
1	1	1	0	CCITT with 300-Hz notch
1	1	1	1	CCITT with 1-kHz notch

Table 4-6 gives the various possible signal paths with the plug-in links in the positions shown in Fig. 4-16.

Under these conditions the signal fed into socket 31 or the demodulated signal follows the following paths on the Filter PC board:

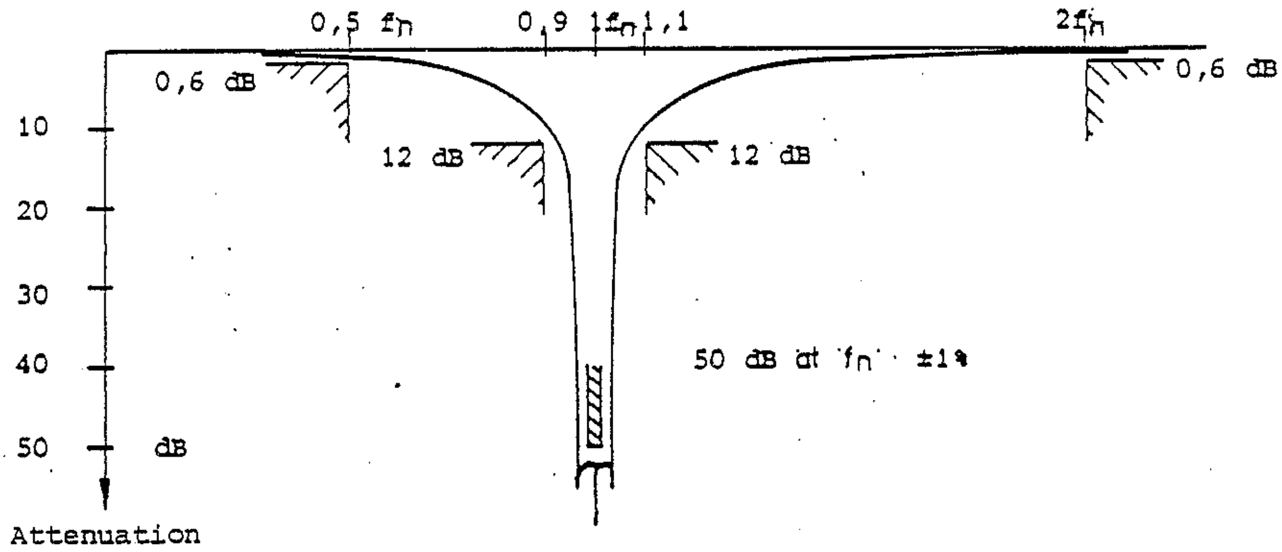
1) Through-connection	when measuring AF or modulation
2) CCITT	when measuring AF or modulation with CCITT weighting
3) Notch filter .3/1 kHz or .5 kHz	alternately with 1) when measuring the distortion (SINAD) of the demodulated signal or of the AF
4) CCITT + notch filter .3/1 kHz or .5 kHz	alternately with 2) when measuring the distortion (SINAD) of the demodulated signal or of the AF with simultaneous CCITT weighting

The CCITT filter is mounted on its own PCB; it is active and weights the signal approximately according to the ear response.

The two notch filters for .3/1 kHz and .5 kHz are of similar design. Only in the .3/1-kHz notch filter the frequency-determining components are switched over to change the notch frequency.

The first stage is an active Wien-Robinson rejection filter. It can handle a voltage of 1 V_{rms}. The notch frequencies are determined by two separate RC voltage dividers, i.e. notch frequency and bridge balance for 1 kHz and 300 Hz can be adjusted independently of each other.

The second and the third stage are identical RLC series-resonant circuits of constant Q. For the filter resistance and filter capacitance the usual passive components are used while the filter inductance is electronically produced by the gyrator circuit B30, B50, B95 or B115. The two notch frequencies of the .3/1-kHz filter can be adjusted practically independent of each other.



Frequency	<fn/2 >2 fn	fn/2 2 fn	0,9 fn 1,1 fn	0,99 fn 1,01 fn
Attenuation	<0,6 dB >0 dB	≤0,6 dB	<12 dB	>50 dB

Fig. 4-17 Standard attenuation characteristic of notch filter

Fig. 4-17 shows the typical attenuation characteristic of the complete filter tuned to the notch frequency f_n.

The table contains the limit values of the minimum and maximum attenuation.

In various models the plug-in links are in a position in which a notch filter can be cut into the signal path instead of the CCITT filters. In these models the components are chosen such that the rejection frequency is at 150 Hz. Under these conditions the signal fed into socket 31 or the demodulated signal follows the following paths on the Filter PC board:

1)	Through-connection	when measuring AF or modulation
2)	Notch at 150 Hz	when measuring AF or modulation with 150-Hz tone suppressed
3)	Notch filter .3/1 kHz	alternately with 1) when measuring the distortion (SINAD) of the demodulated signal or of the AF
4)	Notch at 150 Hz + notch filter .3/1 kHz	alternately with 2) when measuring the distortion (SINAD) of the demodulated signal or of the AF with 150-Hz tone being suppressed at the same time.

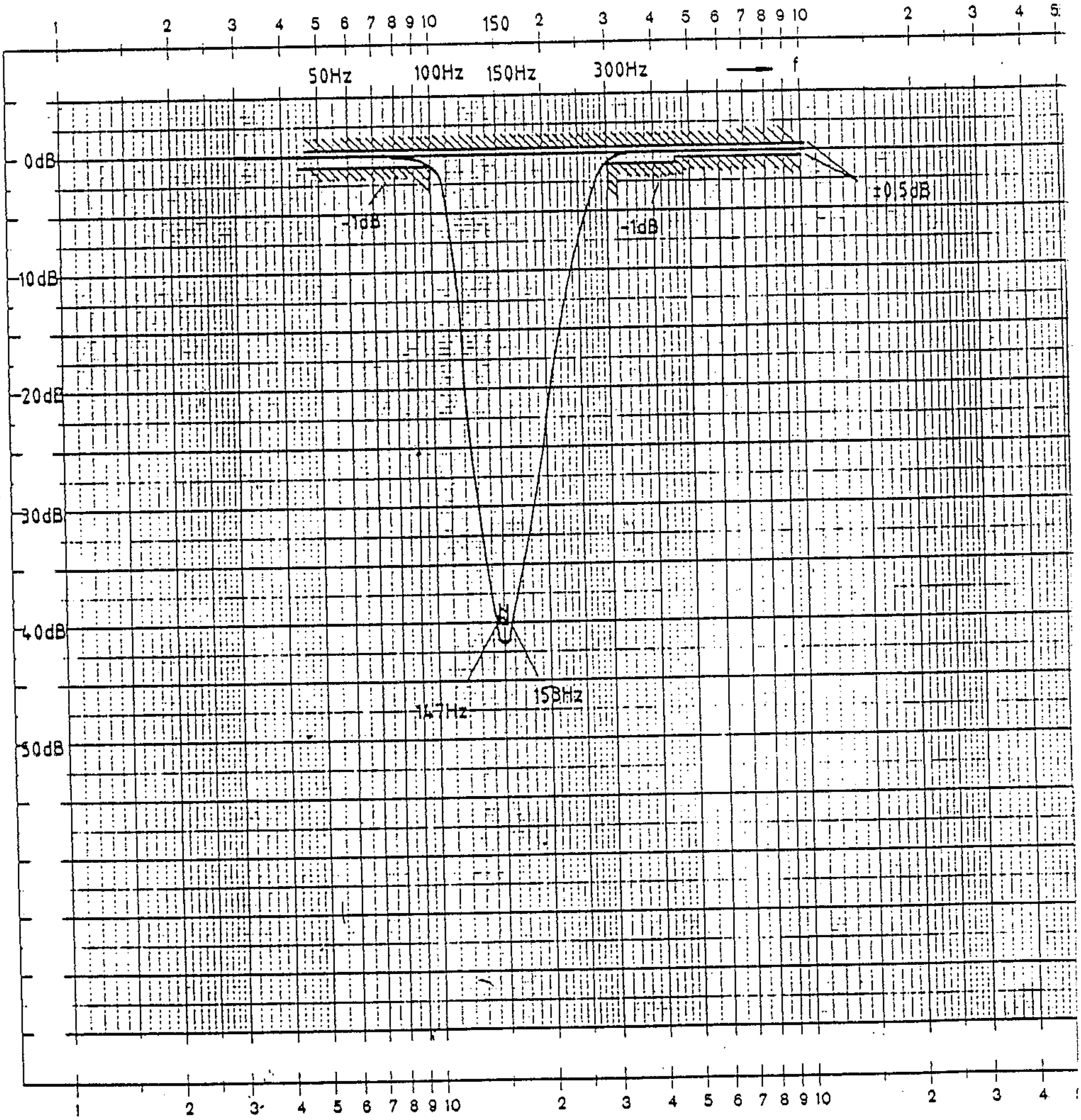


Fig. 4-17.1 Attenuation characteristic of 150-Hz rejection filter

4.3.9 Power Supply

4.3.9.1 DC-DC Converter Y48

(See circuit diagram 332.3414 S)

Power supply

The SMFP2 can be powered from the AC supply or from a battery.

If the SMFP2 is powered from the AC supply, the AC supply voltage is stepped down to a single voltage and rectified (24 V). The DC voltage can, however, also be derived from a battery and can be between 11 and 33 V. It is used for driving a DC-DC converter which delivers the supply voltage for the SMFP2. The SMFP2 requires the following voltages and currents:

+5 V (5 A); +15 V (2 A); -15 V (-1.5 A); +20 V (1 A); +32 V (20 mA).
The voltages +5 V, +15 V, -15 V and +20 V are produced by means of four "forward" converters. The +20-V voltage is chopped and doubled in a "Greinacher" circuit to obtain the required +32-V voltage.

"Forward" converters

All four "forward" converters function according to the same principle, therefore only the 5-V converter is described here.

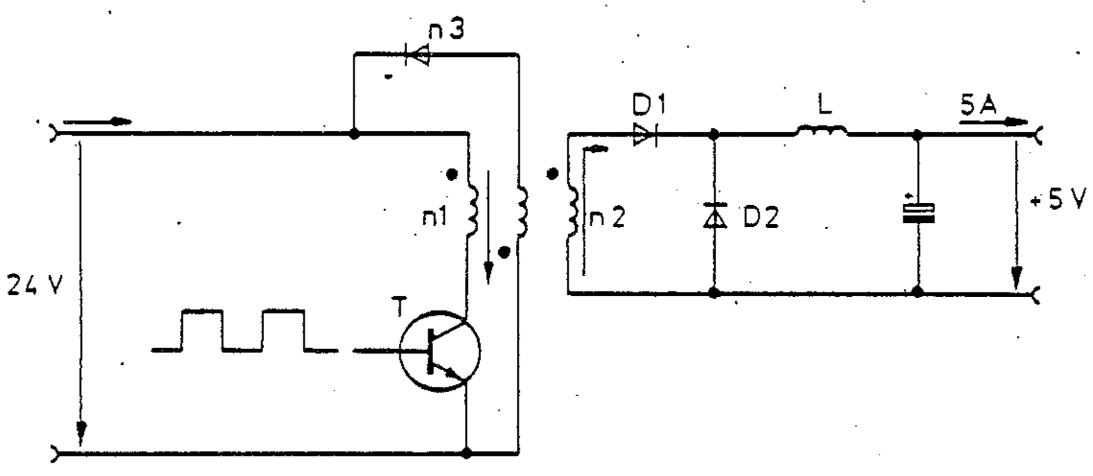


Fig. 4-18 Functional diagram of "forward" converter

During the "on" time of the transistor T, the primary winding n1 and the secondary winding n2 carry current. During the "off" time of the transistor, the inductance L keeps the load current approximately constant which, however, does not now flow through n2 and D1 but through the free-wheel diode.
The control IC B1 (circuit diagram) keeps the output voltage constant at 5 V by varying the duty cycle at a constant switching frequency of about 30 kHz. The IC contains an RC oscillator whose frequency is determined by the external components T2 and C1.

The primary and the secondary side of the converter are isolated from each other which allows either the +pole or the -pole to be grounded when operating from a battery. The reference voltage (GL7,8) is present on the secondary side and because of the isolation, the control signal must be transmitted to the regulator IC via the optocoupler (B10). The transformer winding 7-8 produces an auxiliary voltage for the driver transistor which is equal to about one-half of the primary voltage.

This measure reduces the dissipation of the driver transistor.

TR2, T1 provide short-circuit protection. If a short-circuit occurs on the secondary side, a very high current flows in the winding 1-2, which is measured by TR2. The voltage proportional to the current is rectified reducing the duty cycle via pin 9 (B1).

4.3.9.2 DC Filter Y49

(See circuit diagram 332.3014 S)

The voltages derived from the DC-DC converter are here filtered once more and are now available as supply voltages for all the circuit boards.

4.3.9.3 Regulator Y38

(See circuit diagram 332.2918 S)

The regulator performs three mutually independent functions:

1. It produces voltages which the DC-DC converter does not provide.

   The -5.2-V voltage is derived from the -15-V voltage by means of the integrated voltage regulator B20.

   The stabilized 28-V voltage is derived from the 32-V voltage by means of the stabilization circuit B30, T30.

2. The presence of all the necessary voltages for the SMFP2 is indicated by the LEDs GL20, 32, 50, 52, 54 and GL 56. In addition, a signal is supplied in the case of overvoltage to switch off the SMFP2.

   If the -15-V voltage is exceeded, a current flows at 11a. If any positive voltage is too high, a current flows at 13a.

3. The beat signal from the mixer is amplified in B1 and taken to the headphones via 8b. The same signal is also amplified in B10 and can then be heard over the loudspeaker connected to 9b.

4.4 Digital Section

4.4.1 Computer Board Y21

(See circuit diagram 355.2514 S)

The computer board Y21 carries the 8085 microprocessor and the clock frequency processing circuit. Further subassemblies that are directly connected to the microprocessor via bus and address lines are provided on the following boards:

Ports	on motherboard	III
Display interface 8279 and LCD control	on display board	Y29
Counter output	on counter board	Y33
A/D converter output	on A/D converter board	Y22
AF generator control	on AF generator board	Y24
AF level control	on AF attenuator board	Y23

The microprocessor consists of the CPU	8085	B1
six 8K ROMs with 16 ports each	2764	B7, B8, B9, B10, B11, B12
one 0.25K RAM with 22 ports	8155	B14
one 2K RAM, battery-backed		B13
four interface IC's (8 ports each)		B26, B27, B28, B29

The clock frequency for the microprocessor is derived from the 10-MHz reference frequency from the generator section. The D-type flipflop B3 divides the frequency down to 5 MHz which is taken to the clock input via the driver B2II. The driver B2I is used as a buffer amplifier for the 10-MHz signal for the AF generator. The delay circuit made up of R6, C1 and B2III, IV delays the start of the microprocessor when switching on the AC supply of the SMFP2.

B4, B5 are two-way bus drivers for the data bus or for the external chips.

B6 is used to store the eight low-value address lines for the ROMs and the external chips. The addresses are transferred via the ALE line.

B15, B16, B17 decode the high-value addresses for the memories and the external chips.

The addresses for the external chips are gated with the read or write line via B19, B21, B22, B23, B24 and B25 to obtain read and write addresses.
The external addresses are brought out via the male connector ST21.

Definition of addresses:

ST21:	b32	Y39	$\overline{CS}$
	c20	Y29	$\overline{CS}$
	c19	Y39	Adr
	c29	Y29	Figure
	c28	Y29	Character
	c26	Y29	Keyboard chip A8
	a17, a18, a19, a20	Y33	Counter store
	c13, b13	Y22	A/D converter
	b24, b25	Y24	Adr AF frequency
	c22, c21	Y23	Adr AF level
	a24, a25		Port motherboard
	b20	Y22	Port
	c16	Y24	Adr.

The 8085 microprocessor uses the interrupt lines RST 5.5, RST 6.5 and RST 7.5. RST 5.5 is controlled from the keyboard and RST 7.5 from the RF overload protection circuit.

The ports of ST28 are used for data transmission to the computer Y11.
Pins 9, 10, 11, 12, 13, 14, 15, 16 are assigned to the data lines.
The lines at pins 6 and 7 are handshake lines.

The pins of ST21 have the following functions:

ST21 Pin No.	Board No.	Function
a12	SMFS2B8	Identification
a13	SMFPB61	Identification
b12	Y22	Data valid
c12	Y22	Busy
b22		
b11	Y31	Control indication
c 8	Y39	DMA request
c31	Y39	Trigger
b 9	Y31	Low-pass filter
b19	SMFP-B2	Doubler option identification
b21		RF overload protection
a 8	Y36	300 Hz/1 kHz
c 9	Y39	DMA acknowledge
c11	Y22	Gain 10 dB
c18	Y22	Gain 20 dB
c17	Y22	Gain 20 dB
a27	Y37	Peak value
a26	Y37	Rms value
a28	Y37	Phase
a30	Y37	Power, voltage
a31	Y37	I_{high}, I_{low}
c24	Y23	Range 5/50/500
c25	Y23	
a29	Y33, Y32	f > < 500 MHz
a21	Y33	Clock inhibit
a22	Y33	Reset
a10	SMFPB61	A/D converter on
a11	SMFPB61	Release latch
a 9	Y24	Selective call decoder
b17	Y22	DC switch
c10	Y22	Clock
b10	Y31	Input switch
b26	Y29	OVERFLOW light
b27	Y29	REMOTE light
b18	Y32	Deemphasis switch

ST21 Pin No.	Board No.	Function
a 14	SMFS2B8	Changeover switch
b 14	Y37	Measuring diode
c 14	Y10	AF generator switch
a 16	Y36	500 Hz
b 16	Y24	CCIR/ZVEI

Link 5 is used as an aid in the manufacture of the SMFP2 and should be connected to +5 V during operation.
Link 4 is used as an identification for SMFS2B7.
Link 3 is used as identification for SMFP2B3.

4.4.2 Display Y29

(See circuit diagram 332.5169 S)

The display board consists of two main electrical sections one containing the LCDs and LCD control and the other section the 8279 keyboard chip with keyboard and LED control.

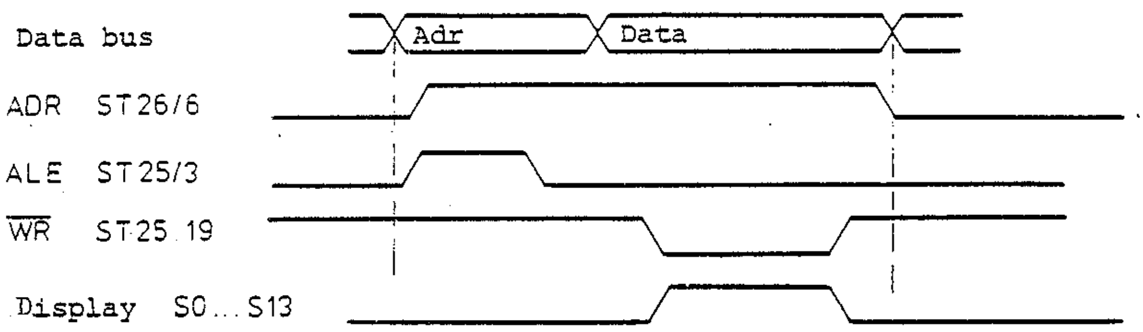
The LCDs B11, B12, B13 and B14 are controlled via the display stores and decoders CD4056 and the display stores CD4054. The figures are controlled by B21 to 28, B32 to 35, B41 to 43, B47 to 50, B53 to 56, B49 to 61 and the units and characters by B29 to 31, B36 to 40, B44 to 46, B51 to 52, B57 to 58, B62 to 65.

The LCDs must be operated from an AC voltage which is produced in the multivibrator B15. The frequency is about 60 Hz. The data for the control elements for the LCDs are supplied directly from the computer bus. The transfer addresses for the figures are decoded via the chips B17II, B16II, B16IV and B18 and for the units and characters via the chips B16II, B17I, B16III and B19.

B80 and B81 are monostables which produce the time delay for the control lines ALE and $\overline{WR}$ of the computer.

In addition, the control of the cursor indication is decoded by the data bus via B67 and the control of the quasi-analog indication (circle) is decoded via B68.

Example of transfer of figures to the displays



The chip 8279 (B9) acts as an interface between the microprocessor and the display or keyboard. The display information is written into the display RAM of the 8279. The contents of the RAM are periodically output to the multiplexed displays under control of the 8279.

SLO to SL3 are the four binary coded control outputs which periodically switch over the display digits. B72 decodes the control outputs and drives the transistors T11 to T16 of the diode groups via the driver B73. In synchronism with the control outputs SLO to SL4, the data for the display digits are output at the data outputs AO to A3 and BO to B3 via the drivers B74, B75.

By decoding the four control outputs SLO to SL3 via B71, a periodic pulse is obtained for scanning the keys. If a key is pressed, the scanning pulse is connected through to tone of the return lines RLO to 7. The information as to which of the eight return lines has been enables is stored in the 8279 where the information on the status of the SL outputs is also stored. From this combined information, the position code of the key is obtained. If a key is pressed, an Interrupt causes the microprocessor to call up the position code stored in the 8279.

Each press of a key causes the 8279 to issue only one Interrupt. If the variation keys are held down, the counter modules B3, 4 produce a periodic check pulse which periodically interrupts the connection of the outputs B36 to the return line inputs RLO to RL7 at gate B8 which is, in effect, like repeatedly pressing the particular key.

The positive check pulse at output 1 of gate B5/I is produced whenever the counter modules B3, 4 have reached the final count. Before any one of the STEP keys is pressed, C1 is charged. B1, B3, B4 are preset via the SET, PRESET, RESET inputs as follows: The outputs Q and $\overline{Q}$ of B1/I and B1/II are at "high" and "low", respectively. B3 is preset to the information at the data inputs, i.e. to 8. B4 is reset to zero. B4 functions as a fixed 10/1 divider. The check output B5/1 is at low.

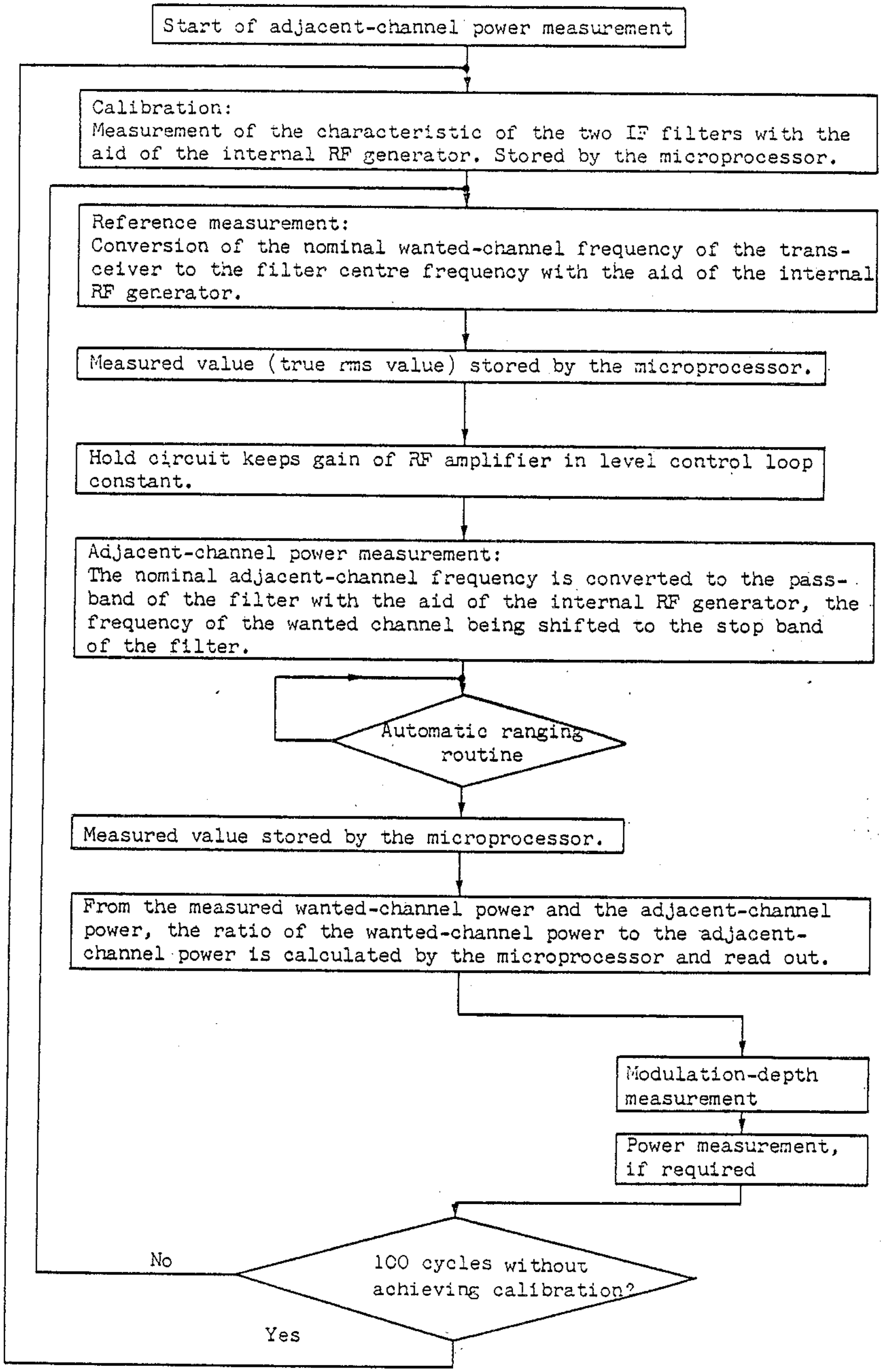
When one of the variation keys is pressed, the negative scanning pulse, which has a repetition period of 5 ms, is connected through to C1 and the count input CK UP of B4. C1 is discharged and the potential at the SET, PRESET, RESET inputs changes. The two cascaded counters are preset to 80. After 80 scanning pulses, corresponding to 400 ms, the counters have reached their final count. The flipflop B1/I is switched over by the positive-going edge of the borrow pulses from B3. This pulse is produced whenever the counters have reached final count. The second borrow pulse switches the Q, $\overline{Q}$ outputs of the flipflop B1/II over to "low" and "high", respectively. After the third borrow pulse, the counter B3 is no longer preset to 8 but to 2. The count cycle is then only 20 scanning pulses corresponding to 100 ms. Thus, with continuous variation, the first four steps take place every 400 ms and all further steps every 100 ms.

4.5 Adjacent-channel Power Meter Option SMFPB61

(See circuit diagram 395.7230 S)

Adjacent-channel power measurement involves the internal RF generator, the RF Amplifier and Mixer board and the Adjacent-channel Power Measurement (NKL) board. The signal arriving from the transceiver is boosted in the RF amplifier to a constant level and is applied to the mixer. The transceiver signal is converted to an IF of 455 kHz in the mixer with the aid of the internal RF generator.

The IF is then applied to the Adjacent-channel Power Meter board where the ratio of the adjacent-channel power to the useful power is determined by the following method.


Start of adjacent-channel power measurement
Calibration:
Measurement of the characteristic of the two IF filters with the aid of the internal RF generator. Stored by the microprocessor.
Reference measurement:
Conversion of the nominal wanted-channel frequency of the transceiver to the filter centre frequency with the aid of the internal RF generator.
Measured value (true rms value) stored by the microprocessor.
Hold circuit keeps gain of RF amplifier in level control loop constant.
Adjacent-channel power measurement:
The nominal adjacent-channel frequency is converted to the passband of the filter with the aid of the internal RF generator, the frequency of the wanted channel being shifted to the stop band of the filter.
Automatic ranging routine
Measured value stored by the microprocessor.
From the measured wanted-channel power and the adjacent-channel power, the ratio of the wanted-channel power to the adjacent-channel power is calculated by the microprocessor and read out.
Modulation-depth measurement
Power measurement, if required
100 cycles without achieving calibration?
No
Yes

The IF at the output of the mixer has a level of approximately 50 mV and is applied via ST9.a to the Adjacent-channel Power Measurement board. The signal is connected through from pin 6 to pin 4 of the analog switch B12 during the test cycles.

During calibration, the signal from the internal RF generator is applied to the signal path via ST341/342 and a 650-kHz low-pass filter. Analog switch B12 then connects pin 7 to pin 4. The following selective amplifier, whose maximum gain is at 455 kHz, features a gain of about 20 dB and a filter Q of about 7.

Whichever of the two mechanical IF filters is required, is connected between ST1 and ST2 into the signal path by means of the relays. The following ceramic filter cuts off the secondary poles of the steel filters.

For wide channel spacing (20 kHz; 25 kHz), the broadband filter (±8 kHz) B1 is used and for narrow channel spacing (10 kHz; 12.5 kHz) the narrow-band filter B2 (±4 kHz).

The circuit element between ST2 and MP4 is a three-stage switchable-gain amplifier. Each stage offers 0 or 10 dB amplification.

Together with the following switchable attenuator, a gain of +30 dB to -40 dB can be accomplished.

B25 constitutes an emitter follower.

Between ST3 and MP10, an rms detector circuit is connected which supplies to MP10 the square of the rms-value of the input voltage (ST3). B6 is a multiplier which is driven with the same signal at both inputs (6, 1).

C32 and B7 act as the integrator of the rms detector circuit. The measured voltage, amplified by a factor of 2, is applied via a 150-Hz low-pass filter (B6) through 12b to the A/D converter.

The circuit element connected between MP10 and ST4a acts as the integrator in the level control loop which keeps the IF at the input of the Adjacent-channel Power Measurement board at a constant level during the reference measurement (wanted channel).

Transistor T12 conducts during the reference measurement. The voltage tapped off from R57 furnishes the reference value for the level control loop which permits setting a constant level as a function of the voltage applied.

If the transistor T12 is turned off, the level control loop is open and the voltage at 4a, i.e. the control voltage for the gain of the RF amplifier, is held at the value previously reached. During this phase, the adjacent channel is measured.

The circuit elements in the large compartment (T15 to T21) and B10 and B11 control the switches along the signal path. Lines b5 to b7 control the amplifier/attenuator in binary code (TTL LLL = -40 dB/TTL HHH = +30 dB). Decoding and control level conversion is accomplished by transistors T17 to T19 and decoder B11.

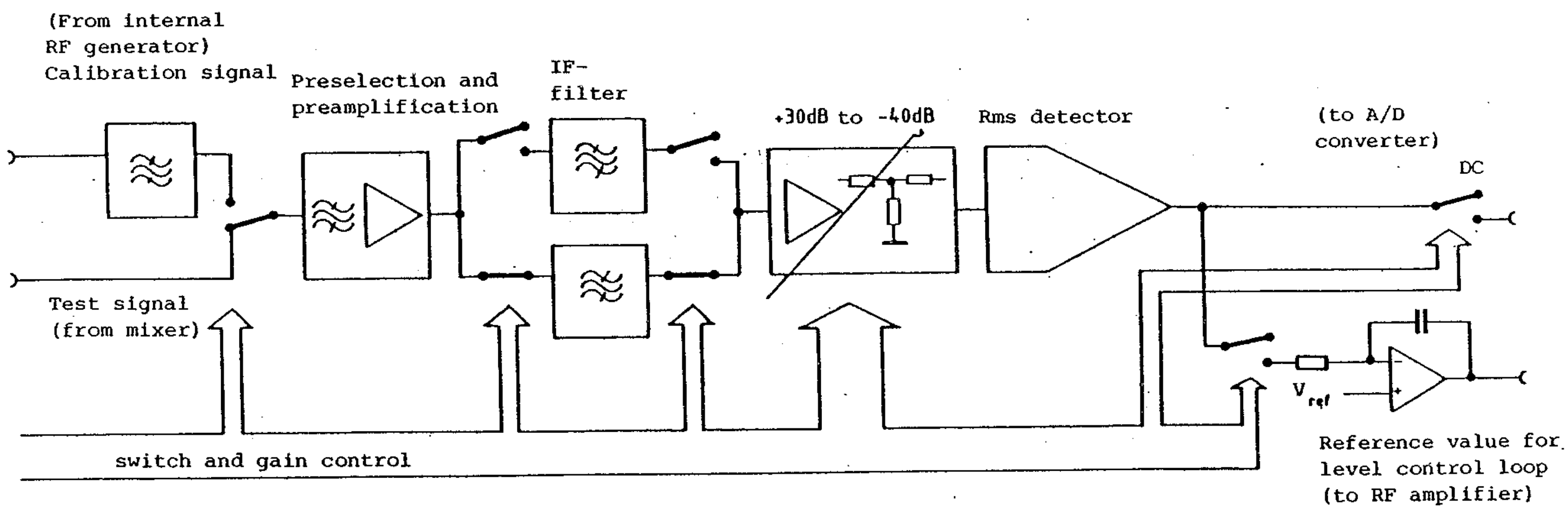


Fig. 4-19 Block diagram of the Adjacent-channel Power Meter Option

4.6 RF Millivoltmeter Option SMFS2B8

(See circuit diagram 332.9312 S)

The operating principle of the RF Millivoltmeter Option SMFS2B8 is based on the comparison of two detector voltages.

Besides the detector circuit for the RF voltage to be measured, the probe and the insertion unit also include a similar detector circuit for the comparison voltage generated in the SMFP2. The difference between the two detector voltages is boosted in the SMFP2. Since the detector voltages may be less than 1 µV, a DC chopper amplifier is provided at the input of the option, consisting of the chopper transistors T45 and T47, the amplifier T50 and B60, the synchronous detector B55 as well as the transistor T65 and the amplifier B70. The generator B40 supplies the switching voltages for the chopper amplifier and the synchronous detector. After amplification the voltage is applied via T80 and T81 to the feedback circuit B25. The transistors T80 and T81 act as a detector which passes positive voltages but rejects negative voltages. This is necessary for a stable control circuit.

The DC output voltage of the transistors T80 and T81 is transformed into an amplitude-proportional 5-kHz squarewave AC voltage in B25. The generator B30 supplies the switching voltage for B25. The transformer TR2 together with the capacitor C20 and the resistors R22 to R24 forms a damped resonant circuit whose resonant frequency is 5 kHz and which transforms the 5-kHz squarewave oscillation into a sinewave voltage. After amplification in the driver amplifier B10 this sinewave voltage is applied via the transformer TR1 to the comparison detector circuit in the measuring head (probe or insertion unit). The gain of the driver amplifier B10 can be varied by means of R21 which is used for setting full-scale deflection on the meter.

Because of the high loop gain of the control circuit, the amplitude of the comparison voltage is adjusted such that the difference between the detector voltages is zero except for a small offset. Since the diodes in the measurement and comparison detector dircuits are selected for identical characteristics, the rms values of the measurement and the comparison voltages are identical if the waveforms are identical (sinusoidal).

The feedback circuit produces proportionality between the output voltage and the rms value of a sinusoidal measurement voltage so that the meter indication is proportional to the rms value of the sinusoidal measurement voltage. The measurement accuracy depends mainly on the degree of uniformity amongst the characteristics of the four diodes used in a measuring head.

The measurement voltage derived from the transistors T80 and T81 is digitally displayed via the relays RS85 and RS86 and the DC voltmeter provided in the basic unit or displayed in analog form on the Analog Display Option SMFS-B9 via connector 4.

5. Repair Instructions

5.1 Measuring Instruments Required

Table 5-1

Ref. No.	Measuring instrument required	Performance specifications	R&S instrument recommended	See section
1	RF counter	Range 0.4 to 520 MHz Resolution 10 Hz	SMFP2/SMFS2 332.0015.52 332.8700.54	5.3
2	Power meter	Range 0.4 to 520 MHz 3 to 20 mW Z = 50 Ω error < 0.1 dB	NRS 100.2433.92	5.3 5.3.10 5.3.12 5.3.15 5.3.16
3	Precision attenuator	Range 0.4 to 520 MHz 0 to 120 dB, Z = 50 Ω	DPVP 214.8017.52	5.3 5.3.17
4	Test receiver Frequency controller	Range 25 to 520 MHz Inherent noise < −10 dB/µV	ESU 2 252.0010... EZK 255.0010...	5.3 5.3.17
5	RF spectrum analyzer	Range 0.4 to 1100 MHz Dynamic range > 70 dB	-	5.3 5.3.11
6	AF generator	Range 50 Hz to 20 kHz Output voltage > 1 V Z_{out} = 600 Ω Distortion < 0.2%	SPN 336.3019.02	5.3.12 5.3.13
7	Test demodulator	RF range 0.4 to 520 MHz AF range 50 Hz to 20 kHz AM 9 to 90% FM 0 to 250 kHz deviation Distortion < 0.2%	FAM 334.2015.53	5.3 5.3.12 5.3.13
8	Distortion meter	Range 50 Hz to 20 kHz Measurement range 0.1 to 10%	FAM + FAM-B8 334.2015.53 334.5714.02	5.3 5.3.12 5.3.13
9	AF counter	Range 0.1 to 1000 kHz Resolution 0.1 kHz		5.3
10	DC power supply	V > 5 V I > 100 mA	NGM 117.7110... or NGR 100.5084...	5.3.15

Ref. No.	Measuring instrument required	Performance specifications	R&S instrument recommended	See section
11	Deviation meter	Range 0.4 to 520 MHz Inherent spurious deviation < 1.5 Hz (CCITT)	FAM + FAM-B6 334.2015.53 334.5614.02	5.3 5.3.18
12	Psophometer	Min. input voltage ≈ 0.1 V with CCITT weighting filter and rms-responding rectifier	UPGR 248.1915	5.3.1 5.3.18
13	Precision RF cable	Z = 50 Ω	SWOB-Z 100.3598.50	5.3.19
14	RF millivoltmeter	Range 1 to 520 MHz Sensitivity ≈ 100 mV	URV 216.3612...	5.3.19
15	RF sweep signal generator with display	Frequency range 30 to 500 MHz Sweep width 2 to 100 MHz Dynamic range > 30 dB EMF 1 V Z = 50 Ω	Polyskop SWOB 5 333.0019	5.3.4
16	Oscilloscope			5.3
17	Digital tester	Indication of high and low TTL level states	–	5.3
18	Service RF adapter for SMS (2)		302.8376	5.3
19	DC voltmeter	Measurement range 0.1 to 50 V R_i > 10 MΩ Error < 0.2%	UDL 4 346.7800.02	5.3 5.3.1 5.3.9 5.3.10 5.3.13
20	AF voltmeter	Measurement range 0.1 to 10 V 50 Hz to 20 kHz Error < 0.5%	–	5.3.9 5.3.12
21	Signature analyzer			5.3.20
22	Power Splitter/ Combiner		DVS 342.1014.50	5.5.9.3

5.2 Troubleshooting

The following flow charts are intended to help determine the faulty circuit board. The figures given in the left-hand section of the boxes refer to the performance checks described in section 5.3. In addition, the numbers of the circuit boards are given on which the fault is to be traced with the aid of the relevant circuit diagram, which specifies the levels and switching states. Prior to trouble shooting, make sure that all supply voltages are o.k. (see section 5.5.8.4).

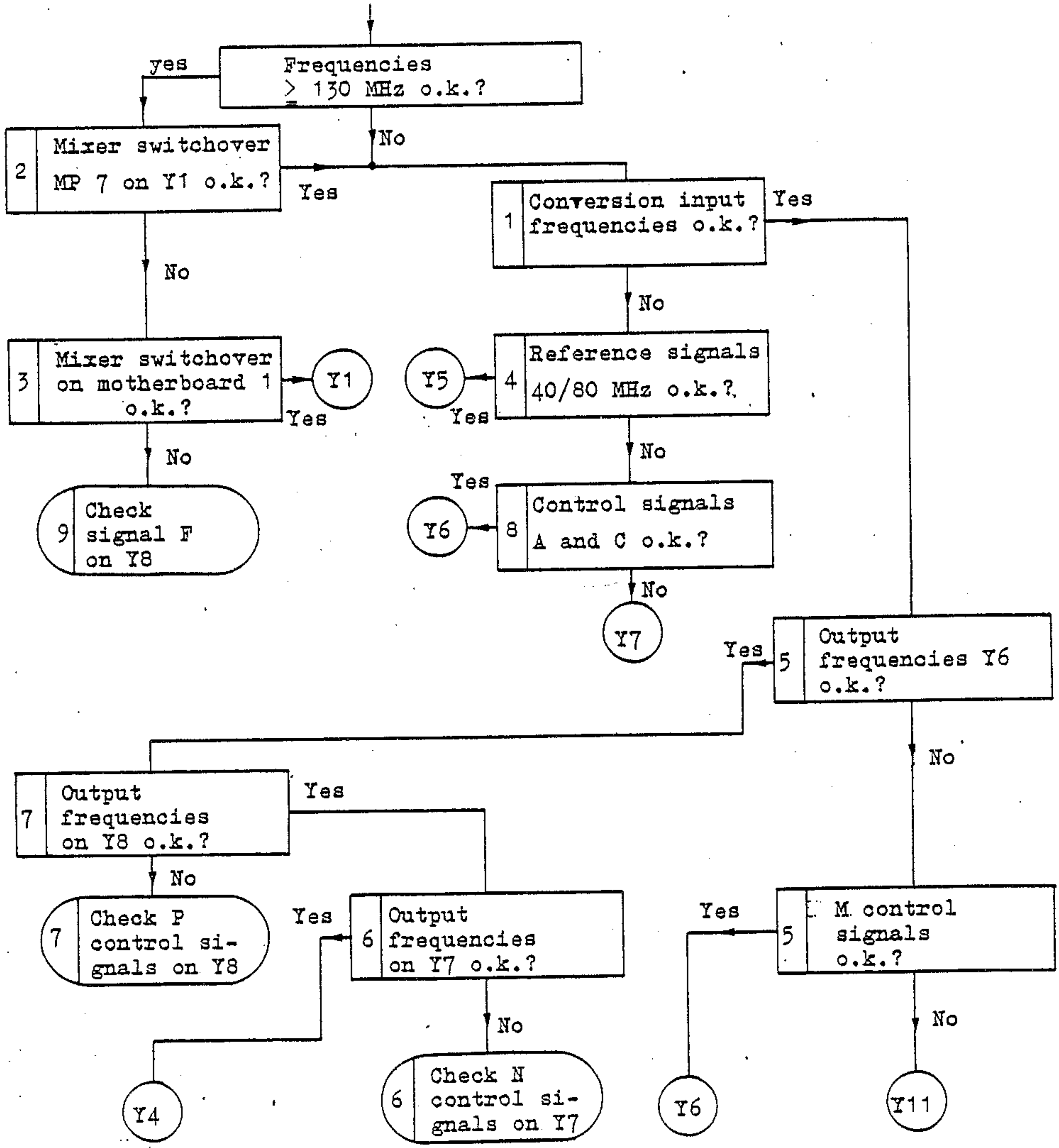
NOTE: Replace circuit boards only with the instrument switched off.

Table 5-2 List of circuit boards

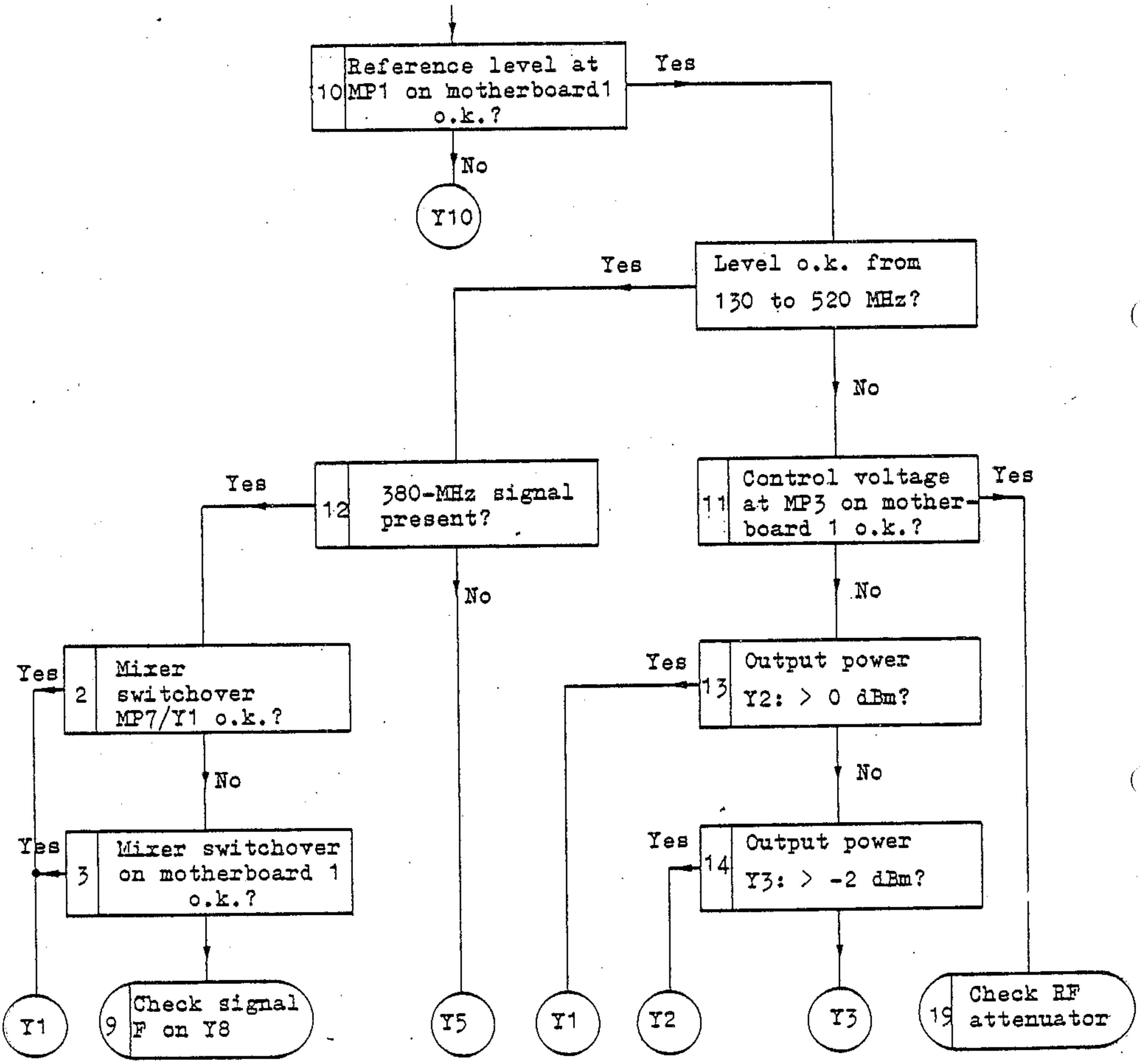
No.	Designation	Id.No.	Colour coding
Y1	Output stage	302.5219	White - white
Y2	Divider	.5419	Green - green
Y3	Oscillator	.5619	Black - black
Y4	Phase control	.5890	Blue - blue
Y5	Converter	.6015	Yellow - yellow
Y6	Reference	.6215	Yellow - red
Y7	50-kHz interpolation oscillator	.6415	Yellow - blue
Y8	100-Hz interpolation oscillator	.6615	Red - red
9	Filter	.6815	-
Y10	Modulation control	.7011	Red - blue
Y11	Microprocessor	.7111	Blue - white
12	Motherboard 1	332.5517	-
13	Motherboard 2	.1040	-
14	Motherboard 3	.3220	-
Y21	Computer board	355.2514	(White - green)
Y22	A/D converter	355.2814	Yellow - green
Y23	Sinewave Shaper	356.5517	Red - green
Y24	Digital section	356.5717	
Y29	Display	332.5169	-
Y31	RF amplifier	.1570	White - black
Y32	Mixer	.1611	Yellow - black
Y33	Counter	.2118	Red - black
Y35	AF amplifier	.2618	Red - white
Y36	Filter	.2799	Blue - black

No.	Designation	Id. No.	Colour coding
Y37	DC amplifier	.2830	Blue - green
Y38	Regulator	.2918	Green - white
Y39	SMFP-B4	.9006.02	Ye-low - red
Y40	Distributor	.3614	-
Y45	RF attenuator for SMFP2	.4010	-
Y46	SMS-B3 overload protection	335.0716	-
Y47	SMFP2 distributor	913.4108	-
Y48	DC-DC converter	332.3414	-
Y49	DC filter	.3014	Blue - blue

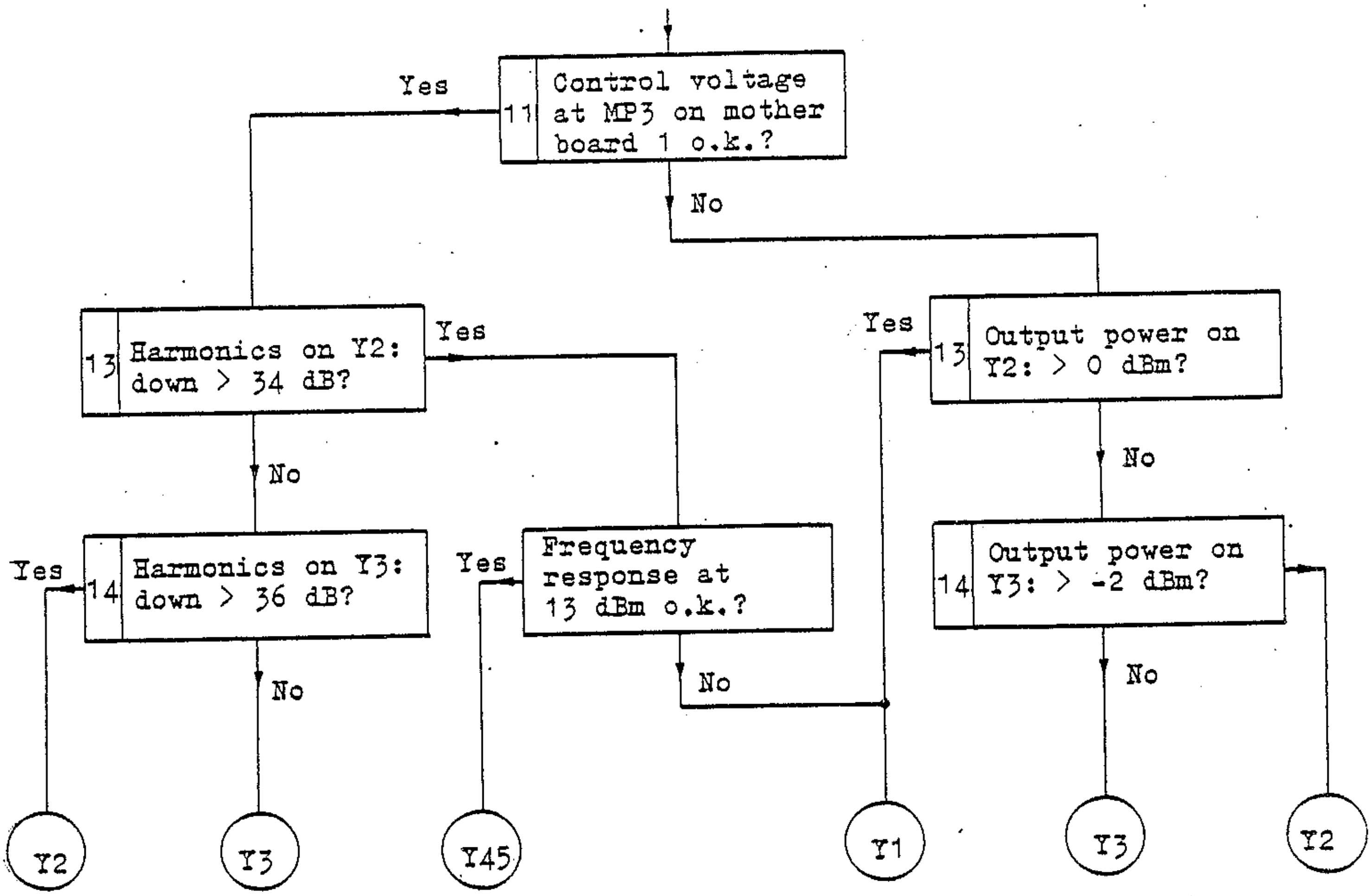
5.2.1 Incorrect Output Frequency



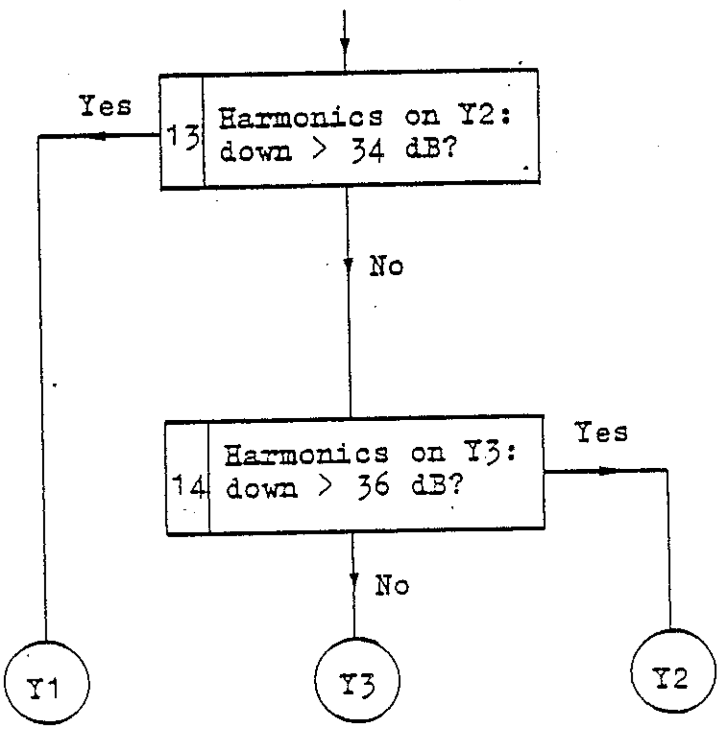
5.2.2 Incorrect Output Level



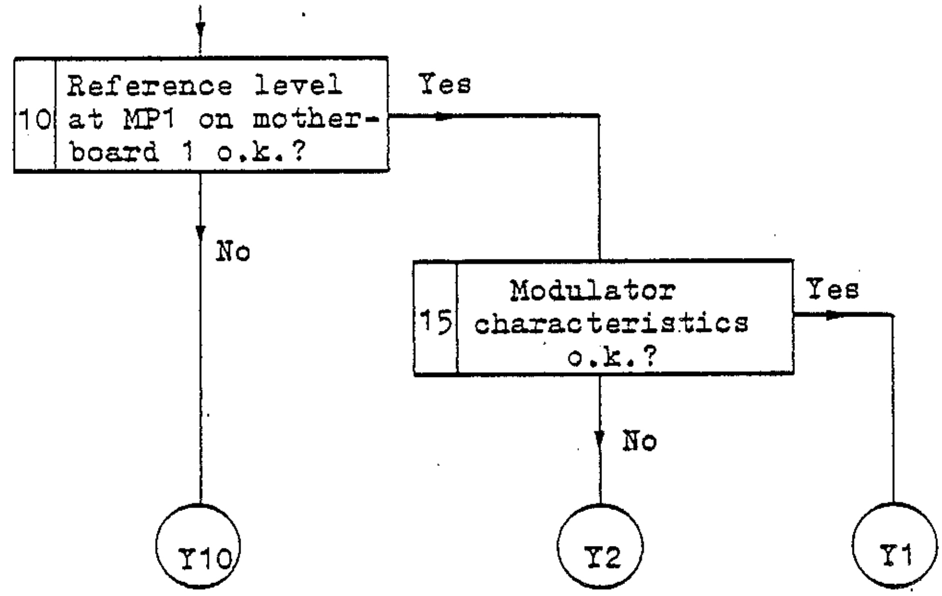
5.2.3 RF Frequency Response not to Specification



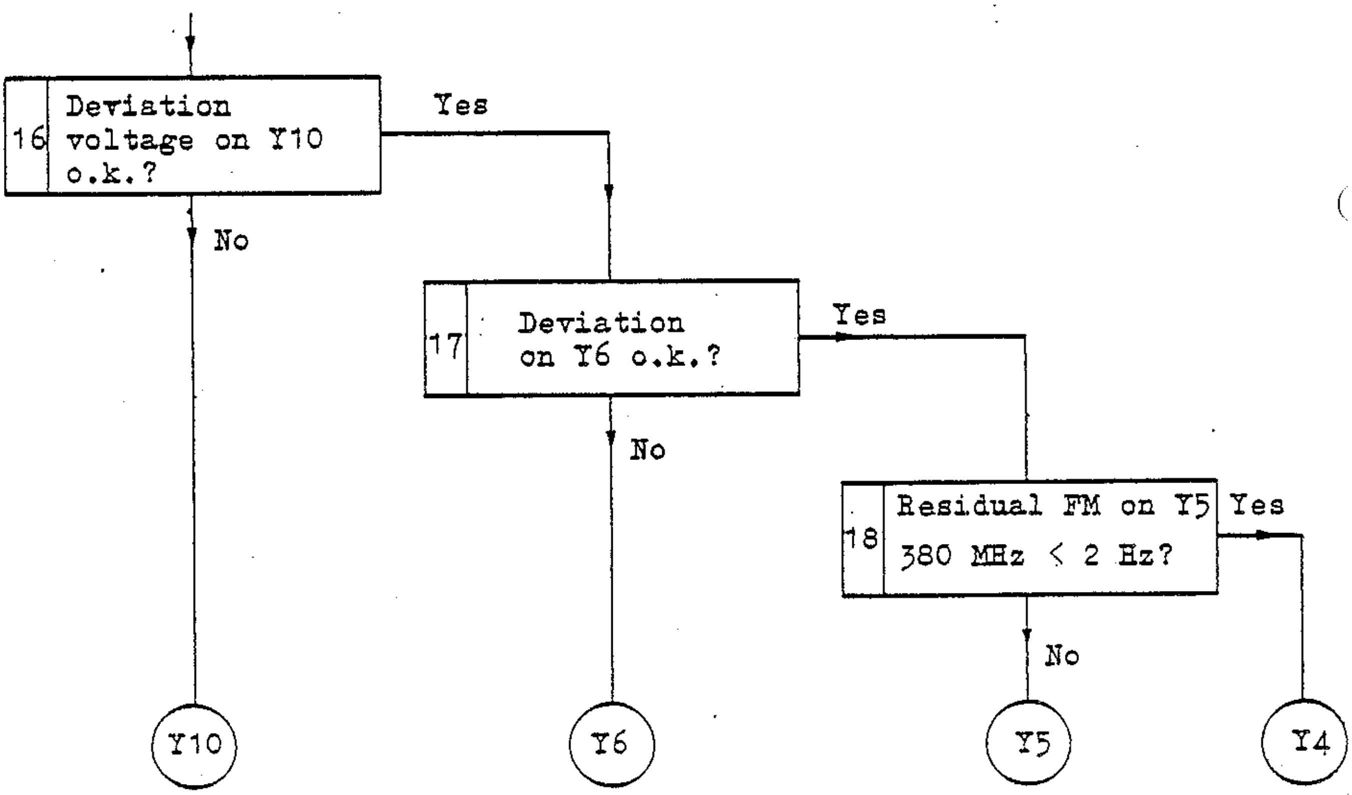
5.2.4 Harmonics not Within Specification



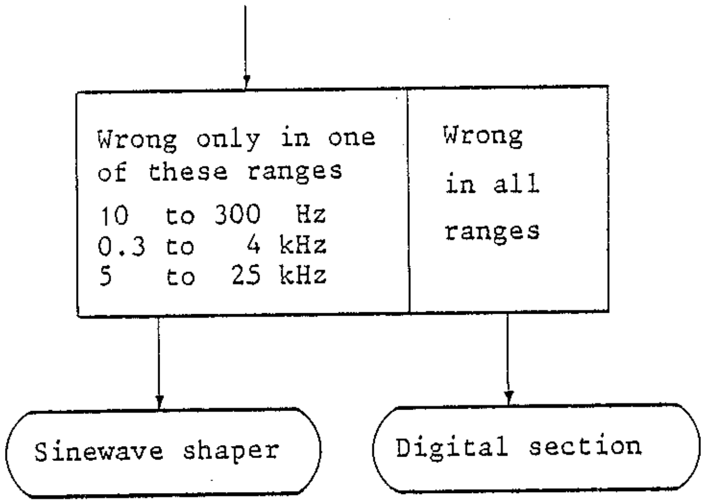
5.2.5 Excessive AM Error or Envelope Distortion



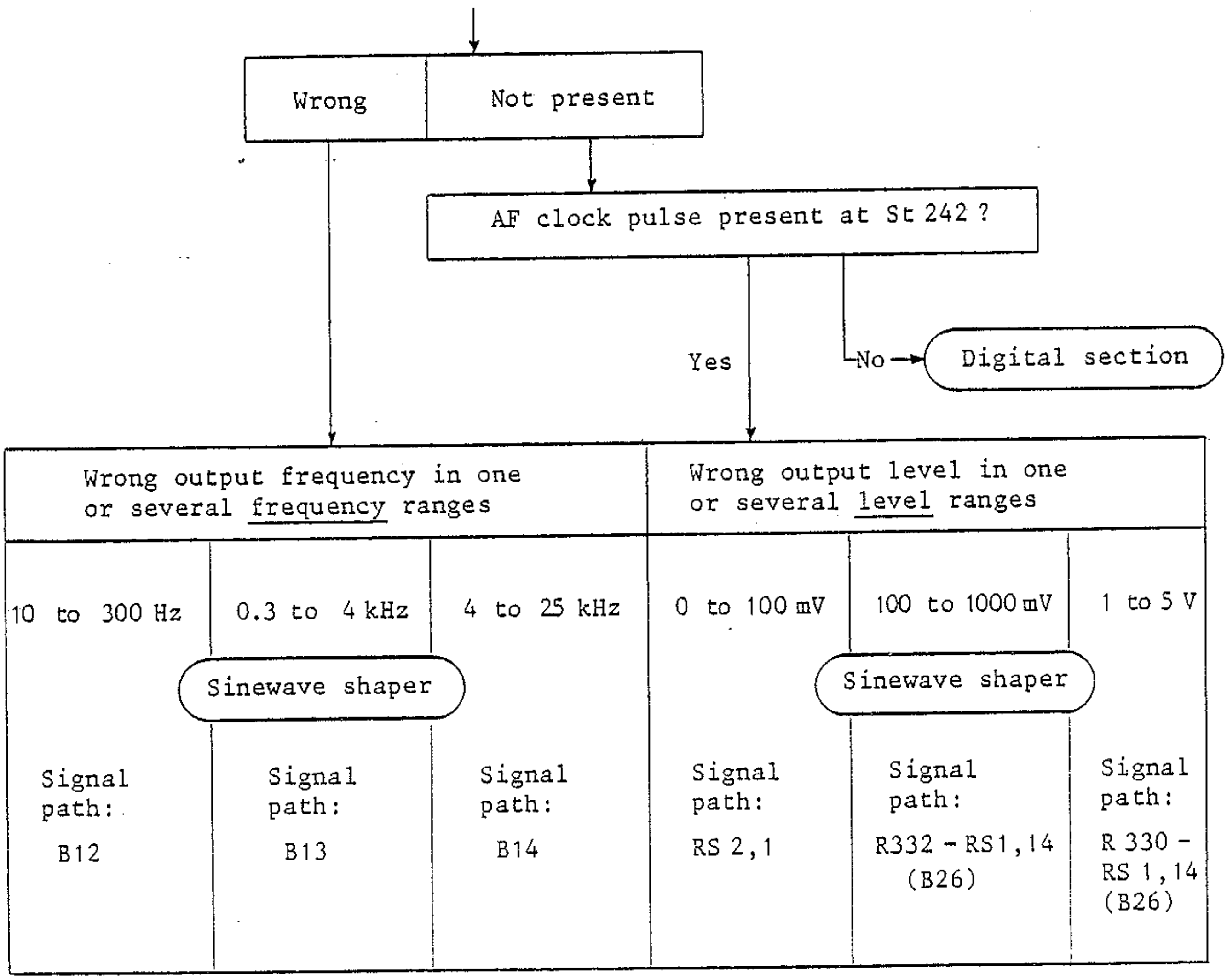
5.2.6 Excessive FM Error of FM Distortion



5.2.7 Incorrect Output Frequency of AF Synthesizer

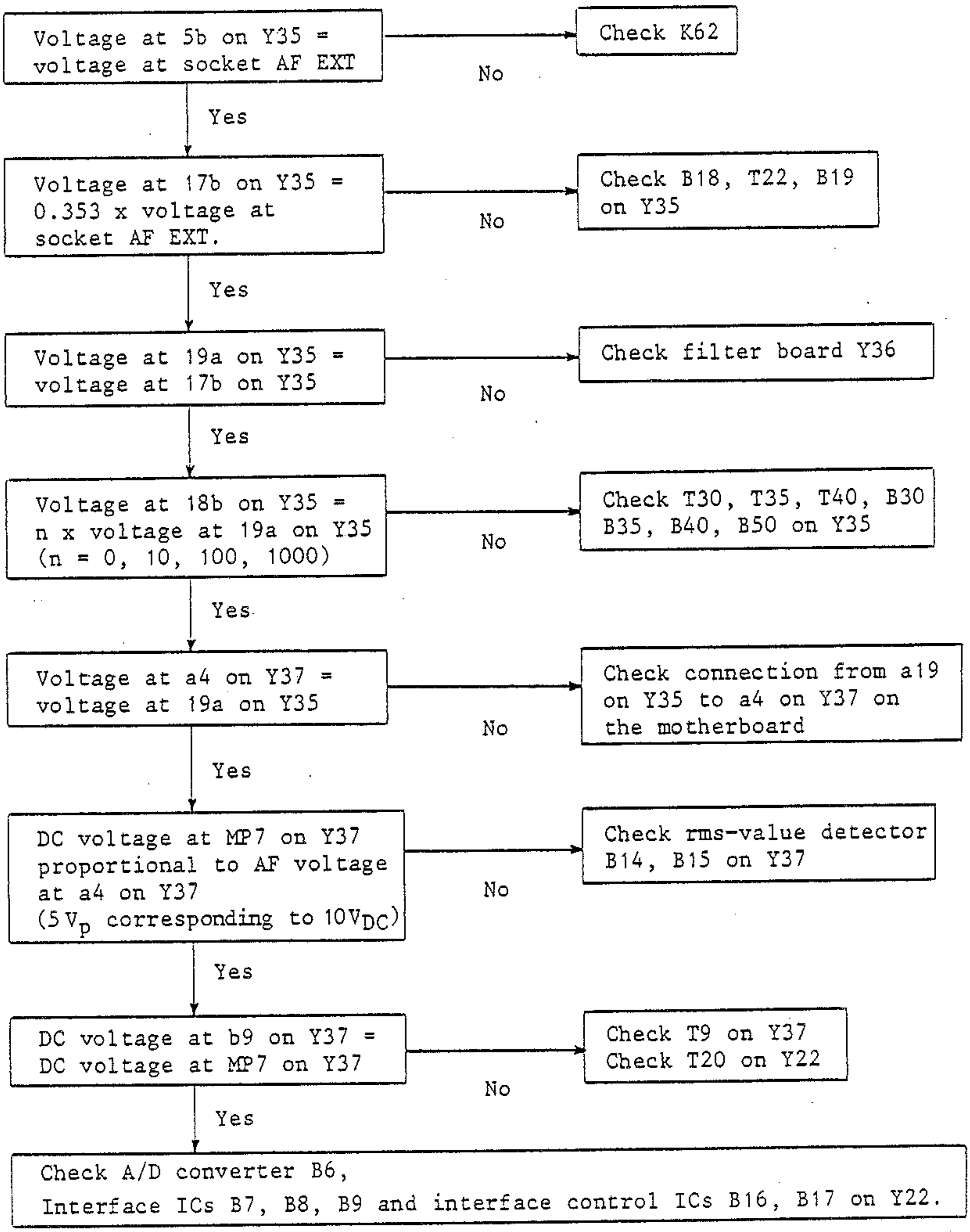


5.2.8 Output Level of AF Synthesizer



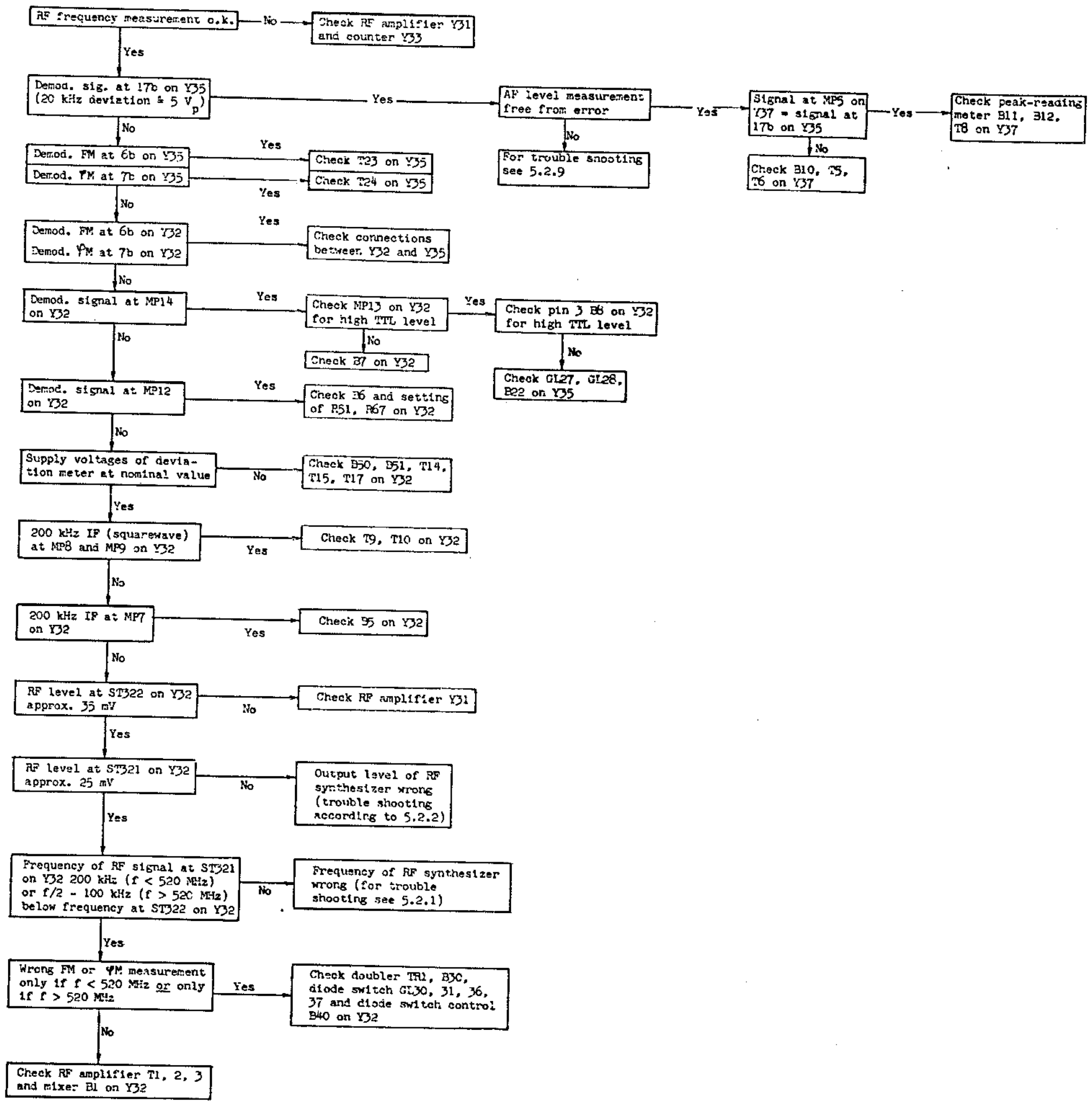
5.2.9 Missing or Incorrect AF Level Measurement

During trouble shooting, no other measurement but the "NF-AC" measurement may be carried out. Switch out the CCITT filter.



5.2.10 Missing or Incorrect FM or φM Measurement

During trouble shooting, no other measurement but the FM or φM measurement and the RF frequency measurement may be carried out.



NOTE: If the FM or φM measurement is wrong only if f > 520 MHz or only if f < 520 MHz, the fault is most likely in the doubler TR1, B30, diode switch GL30, 31, 36, 37 and the diode switch control B40.

5.3 Performance Checks - Generator Section

For certain checks use of a special service adapter is required in order to measure the RF output level and the frequencies of the subassemblies. This service adapter can be obtained from your nearest R&S distributor.

It is also possible to make some of these measurements up to 100 MHz without the use of this service adapter by connecting the frequency counter via a high impedance or using an oscilloscope.

During the measurements, all the circuit boards must always be in operation with the exception of those referred to in sections 5.2.7.1 to 5.2.7.19.

5.3.1 Checking the Conversion Input Frequency

Pull out circuit board Y3. Connect the frequency counter either via oscilloscope probe to BU3/St.19 ab of motherboard 1 or plug the service adapter into the compartment for circuit board Y3 and connect the frequency counter to the RF connector 19. Select frequencies on the SMFP2 and check conversion input frequencies against the following table:

Frequency on the SMF P2	270	300	330	360	390	420	450	480	MHz
Conversion input frequency	300	340	300	340	420	460	420	460	MHz

The signal level of the conversion input frequencies is approximately 25 mV. If the counter sensitivity is inadequate, use an RF preamplifier, such as OM423 Valvo.

5.3.2 Checking the Mixer Switch-over - Circuit Board Y1

Take off cover from circuit board Y1 and plug the circuit board into the adapter. Check voltage at testpoint MP7:

Frequency on the SMF P2	120	130	MHz
Voltage at MP7	+14.5	-14.5	V

5.3.3 Checking the Mixer Switch-over - Motherboard 1

Check voltage at BU1, pin 17b:

Frequency on the SMF P2	120	130	MHz
Nominal voltage BU1, 17b	H	L	

5.3.4 Checking the Reference Signals 40/80 MHz - Circuit Board Y6

Pull out circuit board Y5. Connect the frequency counter either via the oscilloscope probe to BU5/St.11ab of motherboard 1 or plug service adapter into compartment for circuit board Y5 and connect frequency counter to RF connector 11. Select frequencies on the SMF P2 and check reference frequencies against the following table:

Frequency on the SMFP2	270	300	330	360	390	420	450	480	MHz
Reference frequency	80	40	80	40	40	80	40	80	MHz

5.3.5 Checking the M Control Signals and M Divider - Circuit Board Y6

For this check connect frequency counter (Z_{in} > 100 kΩ) which is suitable for processing TTL signals via oscilloscope probe first to MP7 and then to MP8 on motherboard 1. Select frequencies on the SMF P2 against Table 5-3 and check output frequencies. If the output frequencies are incorrect, check the M control signals at BU6 of motherboard 1 against Table 5-3 by means of a TTL digital tester:

Table 5-3

Frequency on the SMFP2 (MHz)	Output frequency (kHz)		M control signals BU6 pin				
	Y8 (MP7)	Y7 (MP8)	13a	15b	15a	17b	17a
280	16.6	16.6	H	H	H	H	L
281	17.2414	17.2414	H	H	H	L	H
285	18.5185	18.5185	H	H	L	H	H
293	21.7391	21.7391	H	L	H	H	H
309	33.3333	16.6667	L	H	H	H	H

5.3.6 Checking the N Divider and N Control Signals

For this check connect frequency counter (Z_{in} > 100 kΩ) which is suitable for processing TTL signals via oscilloscope probe to MP9 on motherboard 1.

Select frequencies on the SMFP2 and check output frequencies against Table 5-4. If the output frequencies are incorrect, plug the circuit board Y7 into the adapter and check the N control signals at the integrated circuit B13 against Table 5-4 by means of a TTL digital tester:

Table 5-4

Frequency on the SMFP2 (MHz)	Output frequency (MHz)	N control signals B13 pin											
		16	15	14	13	17	18	19	20	21	22	23	1
			P7				P6				P5		
445.75	2.145833	L	H	L	L	L	L	L	L	L	L	L	L
445.775	2.147917	L	H	L	L	L	L	L	L	L	L	L	H
445.8	2.15	L	H	L	L	L	L	L	L	L	L	H	L
445.85	2.154167	L	H	L	L	L	L	L	L	L	H	L	L
445.95	2.1625	L	H	L	L	L	L	L	L	H	L	L	L
446.15	2.011538	L	H	L	L	L	L	L	H	L	L	L	L
446.55	2.042308	L	H	L	L	L	L	H	L	L	L	L	L
447.35	2.103846	L	H	L	L	L	H	L	L	L	L	L	L
448.95	2.067857	L	H	L	L	H	L	L	L	L	L	L	L
452.165	2.010313	L	H	L	H	L	L	L	L	L	L	L	L
458.6	2.031579	L	H	H	L	L	L	L	L	L	L	L	L
445.725	2.143750	L	L	H	H	H	H	H	H	H	H	H	H

5.3.7 Checking the P Divider and P Control Signals

For this check connect frequency counter (Z_{in} > 100 kΩ) which is suitable for processing TTL signals via oscilloscope probe to MP10 on motherboard 1.

Select frequencies on the SMFP2 and check output frequencies against Table 5-5. If the output frequencies are incorrect, plug the circuit board Y8 into the adapter and check the P control signals at the integrated circuit B11 against Table 5-5 by means of a TTL digital tester:

Table 5-5

Frequency on the SMFP2 (MHz)	Output frequency (kHz)	P control signals B11 pin											
		P7				P6				P5			
		16	15	14	13	17	18	19	20	21	22	23	1
340.0048	102.4	H	L	L	L	L	L	L	L	L	L	L	L
340.0049	102.45	H	L	L	L	L	L	L	L	L	L	L	H
340.0050	102.5	H	L	L	L	L	L	L	L	L	L	H	L
340.0052	102.6	H	L	L	L	L	L	L	L	L	H	L	L
340.0056	102.8	H	L	L	L	L	L	L	L	H	L	L	L
340.0064	103.2	H	L	L	L	L	L	L	H	L	L	L	L
340.0080	104	H	L	L	L	L	L	H	L	L	L	L	L
340.0112	105.6	H	L	L	L	L	H	L	L	L	L	L	L
340.0176	108.8	H	L	L	L	H	L	L	L	L	L	L	L
340.0304	115.2	H	L	L	H	L	L	L	L	L	L	L	L
320.0024	102.4	L	H	L	L	L	L	L	L	L	L	L	L
399.8727	102.3	L	L	H	H	H	H	H	H	H	H	H	H

5.3.8 Checking the Control Signals A to D - Circuit Board Y7

Select frequencies on the SMFP2 according to Table 5-6 and check the control signals at BU7 on motherboard 1 by means of a TTL digital tester:

Table 5-6

Function	Range identification		Oscillator switch-over	Divider
Control signal	A	B	C	D
Contact	15b	13b	6b	8b
Frequency on the SMFP2 (MHz)				
240 MHz				H
270 MHz	L	L	L	L
300 MHz	H	L	L	
330 MHz	L	H	L	
360 MHz	H	H	L	
390 MHz	L	L	H	
420 MHz	H	L	H	
450 MHz	L	H	H	
480 MHz	H	H	H	
Circuit boards controlled	Y4 Y5 Y6	Y4	Y3 Y4 Y5 Y6 Y10	Y2 Y10

If the control signals are incorrect, successively pull out the controlled circuit boards to check whether the fault is on one of these circuit boards or on circuit board Y7.

5.3.9 Checking the Control Signals E to H - Circuit Board Y8

Select frequencies on the SMFP2 according to Table 5-7 and check the control signals at BU8 on motherboard 1 by means of a TTL digital tester:

Table 5-7

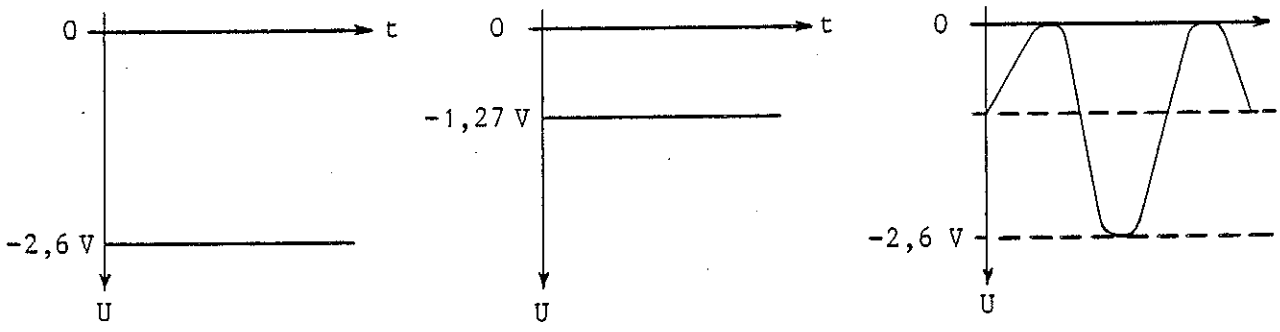
Function Control signal Pin	Filter E 15b	Mixer F 13b	Doubler G 6b	AM slow H 8b
Frequency on the SMFP2 (MHz)				
1		H	L	H
81		H	L	L
161	L	L	L	L
241	H	L	L	L
321		L	L	L
521 *)		L	H	L
Circuit boards controlled	Y2	Y1	Y1 Y10 Range Extension Option	Y1

If the control signals are incorrect, successively pull out the controlled circuit boards and check whether the fault is on one of these circuit boards or on circuit board Y8.

*) Only if fitted with the Frequency Range Extension Option

5.3.10 Checking the Reference Level for Amplitude Control

Connect the oscilloscope to MP1 on motherboard 1 and check the voltage levels:



Unmod. 13 dBm AM 7 dBm, m = 0 AM 7 dBm, m = 100%

If the AM is distorted, check the distortion level (nominal value < 0.3%) of the reference level at MP1.

Settings on the SMFP2: UNMOD., level 13 dBm, frequency 130 MHz.

Set levels according to Table 5-8 by means of 0.1-dB key. Check the voltages at MP1 of motherboard 1. If the voltages are incorrect, plug the circuit board Y10 into the adapter and check the control signals at B25 by means of a TTL digital tester:

Table 5-8

Level on the SMFP2 (dBm)	Level control value Voltage at MP1 (V)	Level attenuator control signal B25 pin						
		P4				P5		
		2	3	4	5	1	23	22
13.0	-2.6	L	L	L	L	L	L	L
12.9	-2.57	H	L	L	L	L	L	L
12.8	-2.54	L	H	L	L	L	L	L
12.6	-2.48	L	L	H	L	L	L	L
12.2	-2.36	L	L	L	H	L	L	L
11.4	-2.14	L	L	L	L	H	L	L
9.8	-1.77	L	L	L	L	L	H	L
6.6	-1.20	L	L	L	L	L	L	H

5.3.11 Checking the Control Voltage

Connect the oscilloscope to MP3 on motherboard 1.

Settings on the SMFP2: UNMOD., level 3 dBm.
frequency 0.4 to 520 MHz.

The control voltage should be between -2 V and -4.6 V over the entire frequency range and should be free from hunting.

5.3.12 Checking the 380-MHz Signal

Insert RF adapter into compartment for circuit board 1. Connect the power meter to RF connector A. The nominal level is between 0.5 and 2 dBm.

5.3.13 Checking Output Power and Harmonics - Circuit Board Y2

Insert RF adapter into compartment for circuit board 1. Connect power meter or RF spectrum analyzer to RF connector 19. Apply DC voltage of -2 V to MP3 on motherboard 1. Check level and harmonics in the frequency range 130 to 520 MHz:

Nominal level:	-4 to +2 dBm
Harmonics (nominal value):	down > 34 dB.

5.3.14 Checking Output Power and Harmonics - Circuit Board Y3

Insert RF adapter into compartment for circuit board Y2. Connect power meter of RF spectrum analyzer to RF connector 4. Check level and harmonics in the frequency range 260 to 520 MHz.

Nominal level:	-2 to +4 dBm
Harmonics (nominal value):	down > 36 dB.

5.3.15 Checking the Modulator Characteristic - Circuit Board Y2

Determine modulator attenuation by measuring the modulator input level (5.2.7.14) and the output level (5.2.7.13) at 260 and 520 MHz with a DC voltage of 0 V, -2 V and -4 V respectively applied to MP3 on motherboard 1.

Table 5-9 Nominal transmission factor (dB)

DC voltage		0 V	-2 V	-4 V	
Frequency	260 MHz	+6.6	+2.4	-10.3	±2 dB
	520 MHz	+5.7	+1.5	-11.5	

5.3.16 Checking the Deviation Voltage

Connect the oscilloscope to MP5 on motherboard 1.

Settings on the SMFP2: FM INT. 1 kHz, deviation 125 kHz, level 3 dBm, frequency 250/260 MHz.

The voltage at MP5 should be 6.2 V_{pp} at 250 MHz and 3.1 V_{pp} at 260 MHz. If the FM is distorted also measure distortion (nominal value < 0.3%) of deviation voltage at MP5.

Settings on the SMFP2: FM INT. 1 kHz, level 3 dBm, frequency 250 MHz.

Set deviation according to Table 5-10. Check the modulation voltages at MP5 of the motherboard 1. If the voltages are incorrect, plug the circuit board Y10 into the adapter and check the control signals at B25 by means of a TTL digital tester.

Table 5-10

Deviation on the SMFP2 (kHz)	Modulation voltage V_{pp} MP5 (V)	Modulation attenuator control signals at B25 pin 20 P6	19	18	17	13 P7	14	15	16
0.5	0.025	H	L	L	L	L	L	L	L
1	0.05	L	H	L	L	L	L	L	L
2	0.10	L	L	H	L	L	L	L	L
4	0.20	L	L	L	H	L	L	L	L
8	0.40	L	L	L	L	H	L	L	L
16	0.80	L	L	L	L	L	H	L	L
32	1.60	L	L	L	L	L	L	H	L
64	3.20	L	L	L	L	L	L	L	H

5.3.17 Checking the Frequency Deviation - Circuit Board Y6

Plug RF adapter into compartment for circuit board Y5.
Connect deviation meter to RF connector 11.

Settings on the SMFP2: FM INT. 1 kHz, deviation 125 kHz,
level 3 dBm, frequency 135/145 MHz.

The output frequencies of circuit board Y6 are 40/80 MHz.
The deviation should be 250 kHz at both settings.

5.3.18 Residual FM of 380-MHz Signal

Plug RF adapter into compartment for circuit board Y5.
Connect deviation meter to RF connector A.

Settings on the SMFP2: UNMOD., level 3 dBm, frequency 260 MHz
Nominal residual FM: < 2 Hz with CCITT weighting filter.

In the FM INT. 1 kHz, deviation 3 kHz mode, the residual FM must not rise.

5.3.19 RF Attenuator

Performance check as described in section 3.2.2.5.

5.3.19.1 Checking the RF Distributor

Prior to the performance check, mount the RF distributor on an appropriately rated heat sink.

Feed an RF signal of, say, 1 W carrier power to E (10 MHz < f < 1000 MHz) 50% modulated with an AF signal of 1 kHz. With the unused RF inputs/outputs terminated with 50 Ω, measure as follows:

at A1: V_{input} -20 dB,
at A2: V_{input} -30 dB,
at A3: V_{input} -20 dB
at the demodulator: 5 V_{peak} 1 kHz AF
(envelopes of V_{input} -20 dB)

The RF distributor is not terminated.

5.3.20 Signature Analysis

Measuring instrument: Signature Analyzer 5004 A from hp.

5.3.20.1 Checking the Microprocessor Board Y11

Setting on the 5004 A:

START edge  , STOP edge  , CLOCK edge  .

Make the following preparations on the circuit board Y11:

- Disconnect the shorting plug from link I and connect to link V.
- Turn the shorting plugs II and III through 90° and engage.
- Connect the START, STOP, CLOCK and GND lines of the 5004 A to the four adjacent test pins ST, SP, CK and ⊥ .
- Switch on SMFP2 power switch 27 (Fig. 2-3).

All signatures that can be measured on the circuit board Y11 are shown on the circuit diagram, e.g. the signature 1FA4 at the output $\overline{WR}$ of B1. The signature at the output port P10 of B1 can be measured if the shorting plug is removed from link V. When checking the signatures, leave all ICs on Y11 and all circuit boards inserted. If an incorrect signature is discovered, proceed step by step to locate the error. First remove all peripheral ICs and then reinsert them one after the other:

- Pull out B2, B5, B13 from Y11.
- Pull out Y4, Y6, Y7, Y8, Y10.
- Disconnect cable connections from the attenuator.
- Check the signatures at the port, bus and control line outputs of B1.

Successively replace B2, B5, B13 and check respective signatures.
After replacing B2, check also the signatures at the port outputs of B2.

One by one insert the circuit boards and reconnect the attenuator each time checking the signatures. The signatures are identical regardless of which circuit boards are in place.

5.3.20.2 Checking the 50-kHz Interpolation Oscillator Y7, the 100-Hz Interpolation Oscillator Y8 and the Modulation Control Y10

Settings on the 5004 A: same as in section 5.3.20.1.
Prepare the circuit board Y11 as in section 5.3.20.1.
Connect START, STOP, CLOCK and GND lines on Y11 as in section 5.3.20.1.
The measurable signatures are shown on the circuit diagrams: input and output ports and CS and PROG. inputs of the input/output expanders 8243.

5.4 Checking and Adjusting the Basic Unit

5.4.1 Microprocessor Y11

For a complete check of Y11 perform steps a) and b) of the test procedures or step c).

a) Checking by entering frequency, modulation, level.
   The display must conform to the entry

b) Checking of control signals for the M dividers at port A of B2 on Y11 against Table 5-11:

Table 5-11

Control signal Pin B2	M0 24	M1 25	M2 26	M3 27	M4 28
Frequency on the SMF P2(MHz)					
280	L	H	H	H	H
281	H	L	H	H	H
285	H	H	L	H	H
293	H	H	H	L	H
309	H	H	H	H	L

Checking of control signals for the attenuator at port B of B2 on Y11 against Table 5-12:

Table 5-12

(UNMOD.) Control signal Pin B2	2 32	4 33	8 34	10 35	20 36	40 37	80 38	100 dB 39
Level on the SMF P2(dBm)								
10 dBm	H	L	L	L	L	L	L	L
8 dBm	L	H	L	L	L	L	L	L
4 dBm	L	L	H	L	L	L	L	L
2 dBm	L	L	L	H	L	L	L	L
-8 dBm	L	L	L	L	H	L	L	L
-28 dBm	L	L	L	L	L	H	L	L
-68 dBm	L	L	L	L	L	L	H	L
-88 dBm	L	L	L	L	L	L	L	H

Checking of control signals I, J, K, M, L, N at port 1 of B1 on Y11 against Table 5-13:

Table 5-13

Control signal Pin B1	I 27	J 28	K 29	M 30	L 31	N 32
Settings on the SMF P2						
50% AM EXT.	H	L	L	L	X	L
50 kHz FM EXT.	L	H	L	L	X	L
50 kHz FM INT. 400 Hz	L	H	H	L	L	L
5 kHz FM INT. 400 Hz	L	H	H	H	L	L
50 kHz FM INT. 1 kHz	L	H	H	L	H	L
UNMOD. RF OFF	L	L	X	H	X	H

For the following measurement, Y7 must be inserted.
Checking of control signals A, B, C, D at BU7 of motherboard 1 against Table 5-14:

Table 5-14

Control signal Contact	A 15b	B 13b	C 6b	D 8b
Frequency on the SMF P2 (MHz)				
300 MHz	H	L	L	L
340 MHz	L	H	L	L
390 MHz	L	L	H	L
135 MHz	L	L	L	H

c) Checking by signature analysis (see section 5.3.20).

5.4.2 Reference Y6

a) 10-MHz crystal oscillator

- BR1, BR2, BR4, BR5 linked.
- Measure frequency at output REF. FREQ. 10 MHz 58 on the rear panel.
- Adjust 10 MHz ± 30 Hz by means of C62.

With the SMFP2 circuit-boards all in place, repeat frequency adjustment to a greater accuracy:

- Connect frequency meter to RF output 48.
- Enter frequency of 520.000 MHz.
- Adjust C62 for 520.0000 MHz ± 250 Hz.

b) Optional 10-MHz reference oscillator (SMS-B1)

- Connect high-impedance DC voltmeter to testpoint MP1. Set minimum DC voltage by means of TR1 and adjust resonant circuit.

Determining the temperature-coefficient turning point of the crystal:

- Connect a frequency meter with a resolution of > 10^{-8} to the socket REF. FREQ. 10 MHz 58 (Fig. 2-4).
- Connect an ammeter in the +15-V voltage supply line (the oven draws approximately 280 mA when cold). After 5 to 10 minutes, the current becomes constant.
- After resistor R52 in steps selected from the E24 standard range between 100 Ω and 500 Ω. Allow about 5 minutes after each change of resistor, then read off frequency.
- Solder in resistor which gives the lowest frequency.

c) 80-MHz oscillator
In addition to board Y6, boards Y7 and Y11 must be in place.

- Enter frequency of 340 MHz.
- Measure frequency at input ST5.11a,b (nominal value 80 MHz).
- By turning coil core of L2, find minimum tuning voltage at MP1. Then turn the coil core clockwise until the tuning voltage is -8 V.

d) Harmonic distortion

In addition to board Y6, boards Y10 and Y11 must be in place.

- Enter frequency of 150 MHz.
- Enter 75 kHz FM INT. 1 kHz
- Measure harmonic distortion at input ST5.11a,b.
- Adjust minimum harmonic distortion by means of R7.
  Nominal harmonic distortion < 1%
  Repeat adjustment under b).

e) Frequency deviation

In addition to board Y6, boards Y10 and Y11 must be in place.

- Enter frequency of 340 MHz.
- Enter 75 kHz FM INT. 1 kHz.
- Measure frequency deviation at input ST5.11a,b.
- Adjust 75 kHz deviation by means of R9.

Checking of control signals M0 to M4 (setting data for M divider) and A, C against Table 5-15:

Table 5-15

Control signal ST6 pin	M0 17a	M1 17b	M2 15a	M3 15b	M4 13a
Frequency on the SMFP2 (MHz)					
280	L	H	H	H	H
281	H	L	H	H	H
285	H	H	L	H	H
293	H	H	H	L	H
309	H	H	H	H	L
Control signal ST6 pin	A 6b	C 8b			
Frequency on the SMFP2 (MHz)					
390	L	H			
300	H	L			

5.4.3 100-Hz Interpolation Oscillator Y8

In addition to board Y8, the boards Y6 and Y11 must be in place.

Coil adjustment:

- Enter frequency of 280.0000 MHz.
- By turning the core of L2, find minimum tuning voltage at MP1. Then turn the core clockwise until the tuning voltage is 4 V ±0.1 V.
- The frequency at input ST7.11a,b is 100 kHz.

Enter frequency of 317.0152 MHz. The voltage at MP1 must be < +25 V. The desired tuning range should be in the centre of the total range available. The frequency at input ST7.11a,b is 134.8 kHz.

Check the output ports P5, P6, P7 of the expander port IC B11 according to Table 5-5 in section 5.3.7.

Check the control signals E, F, G, H of port P4 according to Table 5-7 in section 5.3.9.

Check the input port P2 and the output ports P5 to P7 as well as the inputs CS and PROG. of B11 by signature analysis (see section 5.3.20).

5.4.4 50-kHz Interpolation Oscillator Y7

a) 50-kHz interpolation oscillator

In addition to Y7, the boards Y6 and Y11 must be in place.

Adjustment of coil L6:

- Enter frequency of 297.9901 MHz.
- By turning the core of L6, find minimum tuning voltage at MP1. Then turn the core clockwise until the tuning voltage is 5 ±0.1 V.
- Enter frequency of 318.0001 MHz. The voltage at MP1 should be < +25 V. The desired tuning range should be in the centre of the total range available.

b) Mixer oscillator

In addition to Y7, the boards Y6, Y8, Y11 must be in place.

Adjustment of coil L7:

- Enter frequency of 280.0000 MHz.
- By turning the core of L7, find minimum tuning voltage at MP2. Then turn the core clockwise until the tuning voltage is 5 ±0.1 V.

- Enter frequency of 318.0001 MHz.
- The voltage at MP2 should be +21 V < V < +25 V. The desired tuning range should be in the centre of the total range available.

If the voltage is not within the specified range, correct by readjusting the core.

Check the output ports P5, P6, P7 of the expander port B13 against Table 5-4 in section 5.3.6.

Check the control signals A, B, C, D of the output port P4 against Table 5-6 in section 5.3.8.

Check the input port P2 and the output ports P5 to P7 as well as the inputs CS and PROG. of B13 by signature analysis (see section 5.3.20).

5.4.5 Converter Y5

The circuit boards Y6, Y7, Y8 and Y11 must be inserted.

5.4.5.1 Oscillator Adjustment

Plug RF adapter into the compartment for circuit board Y1.
Connect RF spectrum analyzer or power meter to the RF connector A.

a) Adjust R1 such that the DC voltage at MP1 is about 6.3 V. Connect spectrum analyzer and readjust R1, if necessary, to obtain maximum amplitude and spectral purity.

b) Adjust trimmer C9 such that the phase control activates (output frequency 380 MHz). The tuning voltage at MP6 should be 16 V.

c) By bending the coupling coil L4 set the output level 2 to 4 dBm. Finally, check the tuning voltage and readjust by means of trimmer C9, if necessary.

The setting-up data given are valid with the U-shaped metal shield soldered in place over the oscillator and the circuit board screening closed.

5.4.5.2 Bandpass-filter Adjustment

a) Check bandpass filter switching.
Select frequencies on the SMFP2 and check the switching voltages at MP7 and MP8 against Table 5-16:

Table 5-16

Frequency on the SMFP2 (MHz)	Voltage (V) MP7	MP8
330	+14.5	-14.5
360	-14.5	-14.5
390	+14.5	+14.5
420	-14.5	+14.5

b) Plug the RF adapter into the compartment for circuit board Y6.
Connect sweep generator (SWOB IV) output to RF connector 11.
Remove the mixer B11 from the circuit board Y5 and connect together the socket contacts 1 and 2 with a wire link (0.4 mm dia.).

Insert the second RF adapter into the compartment for the circuit board Y4.
Connect the input of the sweep generator display to RF connector 19.

c) Tune the bandpass filters (with circuit board screening closed) to their resonant frequency according to Table 5-17:

Table 5-17

Sweep range	Frequency setting on the SMF P2	Resonant frequency	Tuning elements
260 to 340	330	300	L26/L27
300 to 380	360	340	L20/L21
380 to 460	390	420	L24/L25
420 to 500	420	460	L22/L23

d) Adjustment of bandwidth and coupling:

To adjust the bandwidth, bend the coupling links between the two coils of the filter. For coupling adjustment, bend the two coupling pins at the ends of the filter coils so as to obtain the attenuation between input and output given in Table 5-18 (RF adapters positioned in the compartments for the circuit boards Y6 and Y3). The attenuation can be directly read off the display screen of the Polyskop SWOB IV if a level reference line is superimposed prior to the adjustment. Since bandwidth and coupling adjustment are mutually interdependent, repeat the adjustment several times. Sweep width is 4 MHz.

Table 5-18

Frequency setting on the SMFP2 MHz	Resonant frequency MHz	Bandwidth MHz	Attenuation dB
330	300	1.5	9 ± 0.5
360	340	1.6	9 ± 0.5
390	420	1.9	9.5 ± 0.5
420	460	2.1	10

The above values are valid if the circuit board screening is closed.

5.4.5.3 Checking the Output Signals

Circuit boards Y5 to Y8 and Y11 must be fitted and the screening closed.

a) Plug the RF adapter into the compartment for the circuit board Y1. Connect the deviation meter (frequency 380 MHz) to RF connector A.

The residual FM of the 380-MHz signal should be
< 1.9 Hz (according to CCITT, rms weighting)
< 8 Hz (50 to 15 kHz, quasi-peak weighting).

b) Plug the RF adapter into the compartment for circuit board Y3. Connect the power meter to RF connector 19. Select frequencies on the Mobile Tester and check the level against the table below.

Frequency on the SMFP2	Level
330	-18 to -22 dBm
360	
390	
420	

5.4.6 Oscillator Y3

a) Setting of operating point and coil adjustment:
In addition to circuit board Y3, the circuit boards Y7 and Y11 must be in place.

- Disconnect link BRI in the tuning voltage line and apply +18.5 V to the oscillator end.
- Enter 300 MHz (oscillator switchover C = low).
- Adjust DC voltage between MP2 and MP3 to 8.5 to 8.6 V by means of potentiometer R2.
- Measure frequency at the RF input ST2.4a,b or at RF output 48 (Fig. 2-3) if the SMFS is fully equipped.
- Adjust 380 ±1 MHz by correcting the spacing of the windings of L6.
- Enter 400 MHz (oscillator switchover C = high).
- Adjust DC voltage between MP1 and MP2 to 8.5 to 8.6 V by means of potentiometer R1.
- Adjust 520 ± 1 MHz by correcting the spacing of the windings of L5.
- Reestablish link connection (BRI) in the tuning voltage line.

For the following checks, the circuit boards Y4, Y5, Y6, Y7, Y8, Y11 must be in place in addition to Y3.

b) Level adjustment:
Measure level at the RF input ST2.4a,b.
Vary frequency by means of keys 22
The RF level should be between -2 dBm and +4 dBm over the frequency range 260 to 520 MHz.
The RF level can be adjusted by correcting the spacing of the coils L6, L8 and L5, L7. This is accomplished by bending L8 and L7, respectively.

c) Enter 260 MHz and 380 MHz and check tuning voltage.
The tuning voltage should be > +2.4 V.

d) Check the stability and spectral purity of the RF signal at the RF input ST2.4a,b in the frequency range 260 to 520 MHz by means of a spectrum analyzer. Check harmonic distortion (down > 36 dB). Adjust R1/R2, if necessary.

e) Measure level at the RF input 20 to 60 MHz (ST4.19a,b). Vary frequency by means of keys 22 over the frequency range 260 to 520 MHz.
The signal level should be > -14 dBm.

5.4.7 Phase Control Y4

In addition to Y4, the circuit boards Y3, Y5, Y6, Y7, Y8, Y11 must be in place.

a) Adjustment of fixed tuning voltages:
Enter the following eight frequencies and adjust voltage at MP5 to 0 ±0.2 V by means of the respective potentiometers (Table 5-19).
For example, enter 270 MHz, vary potentiometer R118 until the voltage at MP5 is 0 V, etc.

Table 5-19

Frequency on the SMFP2	Potentiometer
270 MHz	R 118
300 MHz	R 119
340 MHz	R 120
370 MHz	R 121
390 MHz	R 122
420 MHz	R 123
460 MHz	R 124
500 MHz	R 125

b) Adjustment of residual FM from reference signal.
Enter frequency of 260 MHz. Connect a spectrum analyzer to the RF input ST2.4a,b or, if all circuit boards are in place, to the RF output 48.
Adjust for rejection of the modulation lines 2 MHz and 4 MHz to $\geqq$ 75 dB below the signal by means of potentiomet̀er R83. If no modulation lines are discernible, set R83 to mid-position.

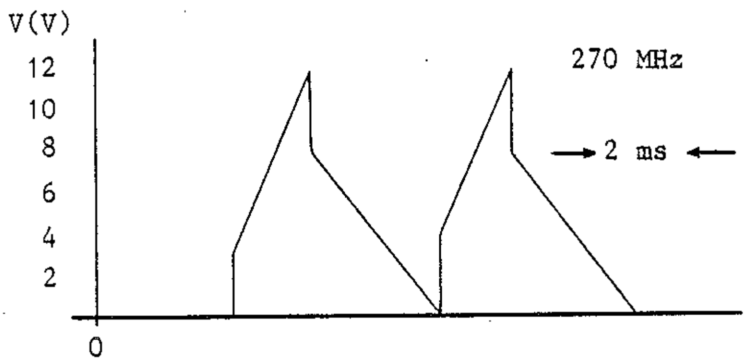
c) Gain switching:
Disconnect the link BR1. Feed in signal (10 kHz, 1 V_{pp}) at test pin of link connected to R92.
Enter frequencies and check voltages at MP6 against Table 5-20.

Table 5-20

Frequencies on the SMFP2	V (V_{pp})
279 MHz	0.14
319	0.14
321	0.20
361	0.27
399	0.13
439	0.13
441	0.16
481	0.22
500	0.42
520	0.62

d) Lock-in aid:

- Pull out circuit board Y3.
- Enter frequencies 270 MHz and 340 MHz.
- Measure signal at MP5.



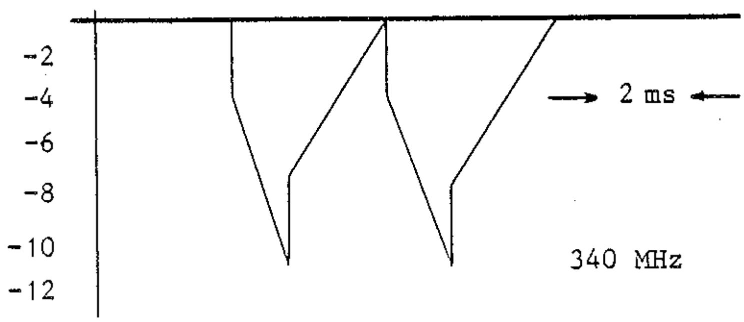


Table 5-21

Control signal ST4 pin	A 6a	B 8a	C 8b
Frequency on the SMFP2			
270 MHz	L	L	L
300 MHz	H	L	L
340 MHz	L	H	L
390 MHz	L	L	H

Table 5-22

Control signal ST4 pin	M0 17a	M1 17b	M2 15a	M3 15b	M4 13a
Frequency on the SMFP2					
280 MHz	L	H	H	H	H
281 MHz	H	L	H	H	H
285 MHz	H	H	L	H	H
293 MHz	H	H	H	L	H
309 MHz	H	H	H	H	L

5.4.8 Checking the Modulation Control Y10

The circuit board Y11 must be in place.

a) Settings on the SMFP2: FM EXT. deviation 100 kHz, frequency 250 MHz.
Connect an AF voltmeter to MP15/Y10.
Apply a voltage of approximately 0.57 V/1 kHz to the modulation socket 39 on the front panel so that the AF voltmeter reads 1.00 V.

b) Adjust deviation and check voltage on the AF voltmeter against the following table:

Deviation (kHz)	9	16	16.5	17	18	20	24	32	64	
Voltage (V)	0.09	0.16	0.165	0.17	0.18	0.20	0.24	0.33	0.64	±1%

c) Settings on the SMFP2: FM EXT. deviation 100 kHz, frequency 260/520 MHz. The AC voltage at MP14 should be 0.50 V.

d) Settings on the SMFP2: UNMOD. level 13 dBm, frequency 130 MHz. Adjust voltage at MP14 to 2.50 V by means of R76.

e) Reduce the level by means of 0.1-dB key and check voltage at MP14 against the following table:

Level (dBm)	12.9	12.8	12.6	12.2	11.4	9.8	6.6	
Voltage (V)	2.47	2.44	2.38	2.27	2.06	1.70	1.15	±1%

5.4.9 Adjusting the RF Level - Y10 and Y2

The circuit boards Y2 to Y8, Y10 and Y11 must be in place.

a) Setting the operating points of the transistors T3 and T4 on the circuit board Y1:
Plug the circuit board Y1 into the adapter.
Adjust the voltage at MP9 to 0.7 V by means of R36 and the voltage at MP10 to 1.3 V by means of R51. (Switch on SMFP2 only for a short time, since, when the cover is open, there is no heat dissipation for T3 and T4)
After adjustment, replace screening cover, screw it on and reinsert circuit board into the cassette without the adapter.

b) Settings on the SMFP2: UNMOD. level 13 dBm, frequency 130 MHz. Set the level to 13.00 dBm by means of R76/Y10.

c) Settings on the SMFP2:FM EXT. level 13 dBm, frequency 130 MHz. Set the level to 13.00 dBm by means of R71/Y10.

d) Adjust frequency to 520 MHz. Set the level to 13.05 dBm by means of C64/Y1.

e) Checking the control voltage:
Settings on the SMFP2: UNMOD. level 3 dBm.
Connect the oscilloscope to MP3 on motherboard 1. The control voltage should be between -2 V and -4.6 V in the frequency range 0.4 to 520 MHz. If the control voltage falls below -2 V, check the output power on the circuit board Y3 (section 5.3.14) and the modulation characteristic on the circuit board Y2 (section 5.3.15).

5.4.10 Adjusting for Minimum Level of Harmonics and Non-harmonic Spurious Signals

All circuit boards must be in place.

a) Connect the RF spectrum analyzer to the RF output 48 of the SMFP2.

b) Settings on the SMFP2: UNMOD., level 3 dBm.
Adjust for minimum level of harmonics in the frequency range 250 to 270 MHz by means of R51/Y1. Check harmonics over the entire frequency range from 0.4 to 520 MHz. The typical value is down > 36 dB.

c) Adjust for minimum level of non-harmonic spurious signals
380 MHz - 2 f_{SMFP2} and
380 MHz - 3 f_{SMFP2} in the frequency range 100 to 129 MHz by means of C91/Y1.
Check non-harmonic spurious signals over the entire frequency range from 0.4 to 520 MHz.

Typical values:	0.4 to 105 MHz	> 70 dB
	110 to 129 MHz	> 65 dB
	130 to 520 MHz	> 75 dB.

To adjust C91, unscrew the left-hand side strip and push down until a hole through which C91 is accessible is visible in the cassette.

5.4.11 Adjusting the Amplitude Modulation

All circuit boards must be in place.

a) Settings on the SMFP2: AM EXT., m = 85%, level 7 dBm, frequency 130 MHz.
Apply external modulation voltage of 1.00 V/1 kHz to the modulation socket 39 (Fig. 2-3). Connect test demodulator to RF output 48 of the SMFP2 (for test set-up see section 3.2.2.10).

b) Set m = 85% by means of R79/Y10.

c) Set level on SMFP2 to 5.1 dBm and reduce to -4.9 dBm by means of 0.1-dB key.
Set m = 85% by means of R101/Y1.

d) Repeat steps a) to c).

e) Settings on the SMFP2: UNMOD., level 13 dBm, frequency 130 MHz.
Connect power meter to the RF output 48 of the SMFP2 and check the level.
Correct by means of R76/Y10, if necessary.

f) Settings on the SMFP2: AM EXT., m = 0, level 5.1 dBm, frequency 130 MHz. Reduce level to -4.9 dBm by means of the 0.1-dB key. Check the level. Permissible deviation ±0.3 dB. If the level unintentionally drops below -4.9 dBm, readjust level to 5.1 dBm and reduce again to -4.9 dBm.

   In the case of greater deviations, adjust R102/Y1 and repeat steps a), b) and e).

g) Check AM error and envelope distortion in accordance with sections 3.2.2.11 and 3.2.2.12, respectively.

5.4.12 Adjusting the Frequency Modulation

a) Settings on the SMFP2 : FM EXT., deviation 75 kHz, level 3 dBm, frequency 390 MHz. Test setup as in section 3.2.2.10. Set modulation voltage (1 kHz) so as to obtain 75 kHz deviation.

b) Adjust R7/Y6 for minimum distortion.
   Correct tuning voltage of circuit board Y6 in accordance with section 5.4.2 b).

c) Settings on the SMFP2 : FM EXT., deviation 100 kHz, level 3 dBm, frequency 500 MHz.
   Apply external modulation voltage of 1.00 V/1 kHz.
   Adjust R9/Y6 for 100 kHz deviation.

d) Set the frequency of the SMFP2 to 460 MHz.
   Adjust R9/Y6 for 100 kHz deviation.

e) Check the FM error and FM distortion in accordance with sections 3.2.2.9 and 3.2.2.10.

5.4.13 Adjusting the Doubler of the 1-GHz Frequency Extension Option SMFP-B2

a) Settings on the SMFP2: level 7 dBm, UNMOD., frequency 750 MHz.
   Set RF level to 7 dBm by means of potentiometer R14 on the circuit board 335.0368 (switch). Measure level at RF output of the signal generator using a power meter. The frequency response of the output level between 520 and 1040 MHz should be flat within ±1 dB. The control voltage at testpoint MP3 of the motherboard 1 should be between -2 V and -4.8 V and must be free from hunting.

b) Settings on the SMFP2: level 13 dBm, UNMOD. and
level 7 dBm, AM INT. 1 kHz, m = 0%.

For the frequencies 520.0001 to 1040 MHz, adjust the level of non-harmonic spurious signals down to > 20 dB by means of potentiometer R13 on the circuit board 335.0316 (doubler).

c) Settings on the SMFP2: AM EXT. 60%, level 7 dBm.
Feed modulation signal of 1.0 V_{rms} to modulation socket. Adjust potentiometer R23 on the circuit board 335.0368 (switch) such that the modulation depth for the modulation frequency range 50 Hz to 20 kHz fluctuates less than ±5%.

5.4.14 Checking the Frequency Setting

Perform check as described in section 3.2.2.2.

5.4.16 Checking the RF Response

The frequency response is preset under section 5.4.2. After level and modulation adjustments, check the frequency response (section 3.2.2.3) and correct, if necessary, by means of C64/Y1.

5.4.17 Checking the RF Attenuator Error

Perform check as described in section 3.2.2.5.

5.4.18 Checking the Spurious Deviation

Perform check as described in section 3.2.2.14.

5.4.19 Checking the VSWR

Perform check as described in section 3.2.2.16.

5.4.20 Checking and Adjusting the AF Synthesizer

5.4.20.1 Digital Section

Checking the reference frequency and the output frequency:

The voltages and logic levels at the test points and connectors are as follows:

AT connector 241	10 MHz TTL
Pin 1, 16 at B12	100 MHz ECL
MP5 approx.	10 MHz TTL
Connector 241	TTL frequencies:
	f x 128 with f = 10 Hz to 300 Hz
	f x 64 with f = 300 Hz to 4 kHz
	f x 32 with f = 4 kHz to 25 kHz,

where f are the frequencies that can be programmed on the front panel.

Checking the programmable divider

Set the frequencies on the front panel according to Table 5-23 and check the output frequencies at ST242 by means of a counter. The formula for the generation of the AF clock at ST242 is given by

$$P = \frac{100\ 000\ 000}{C1}, \text{ where}$$

P = setting of the programmable divider

C1 = frequency of the AF clock at ST242. In the range f = 10 to 300 Hz it is higher than the frequency set on the front panel by a factor of 128; in the range 0.3 to 4 kHz it is higher by a factor of 64 and in the range f > 4 kHz by a factor of 32.

From P the settings of Table 5-23 are obtained according to the following rule:

T = tens: With the tens at MP26 to 38, Z-1 is a binary number.

U = units: With the units at MP18 to 25 and MP39, U is fully decoded.

D = decimals: With the decimals at MP10 to 17, 0.4 x 256 is a binary number.

Table 5-23 Divider control signals

AF clock (ST 242) (Hz)	Programmed frequency (Hz)	Tens Test points: 38	37	36	35	34	33	32	31	30	29	28	27	26	Units Test points: 22	23	24	25	18	19	20	21	39	Decimals Test points: 17	16	15	14	13	12	11	10
2 432	19.0	H	L	L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	L	L	H	H	L	H	H	L	L
2 444.8	19.1	L	H	H	H	H	H	H	H	H	H	L	L	H	H	H	H	L	L	L	L	L	L	L	L	H	L	L	H	L	L
4 876.8	38.1	L	H	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	H	L	L	L	L	L	L
4 889.5	38.2	L	L	H	H	H	H	H	H	H	H	H	L	L	H	L	L	L	L	L	L	L	L	H	L	L	H	L	L	H	L
9 740.8	76.1	L	L	H	L	L	L	L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	H	L	H	L	L	L	L	L
9 753.6	76.2	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	L	L	H	H	L	L	L	L
19 481.6	152.2	L	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H	L	L
19 494.4	152.3	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L	H	H	H	L
38 905.6	607.9	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	H	H
38 912	608.0	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	H	H	H
77 504	1 211	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	H	L
77 568	1 212	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	H	H	L	L	L	H
153 792	2 403	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H	H
153 856	2 404	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	L
303 008	9 469	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
303 040	9 470	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
588 160	18 380	L	L	L	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
588 480	18 390	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	L
302 080	9 440	L	L	L	L	L	L	L	H	L	L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L
301 184	9 412	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L
300 288	9 384	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	H
299 392	9 356	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H
298 496	9 328	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	H	H
297 600	9 300	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	L
296 704	9 272	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L	L	L	L	L	L	H	L	L	H
295 840	9 245	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	L	L	L	L	L	L	H	L	H
294 976	9 218	L	L	L	L	L	L	L	H	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	H	H

5.4.20.2 Adjusting the Sinewave Shaper

Offset adjustment:

- Enter 150 mV.
- Insert BR1 into ⊥.
- Connect DC voltmeter to MOD. GEN. output.
- Adjust R321 until 0 V DC ±1 mV is obtained.
- Change connection of BR1 again.
- Adjust R301 until 0 V DC ±1 mV is obtained.

Gain adjustment:

- Enter 1000 mV, 150 Hz.
- Connect AC voltmeter to MOD. GEN. output.
- Adjust R231 until 1000 mV AC is obtained.
- Enter 1 kHz.
- Adjust R251 until 1000 mV AC is obtained.
- Enter 10 kHz.
- Adjust R271 until 1000 mV AC is obtained.

5. 4.20.2.1 Checking the Sinewave Shaper

Checking frequency range switching:

Programmed frequencies	Logic levels at a12	a13
150 Hz	L	L
1 kHz	L	H
10 kHz	H	L

5.4.20.2.2 Checking the Programmable D/A Converter

Checking the output attenuators and level control signals.

Set levels given in Table 5-24 on the AF Synthesizer Option and measure the AC voltage at the MOD. GEN. front panel socket 34 using a digital voltmeter. If the levels are incorrect, plug the sinewave shaper into the adapter board and check the control signals at the pins of B19 and B18 specified in Table 5-24.

Table 5-24

Programmed voltage on AF Synthesizer	B19										B18	
											LSB	MSB
	13	12	11	10	9	8	7	6	5	4	2	3
4995 mV	H	H	H	L	L	H	H	H	H	H	H	L
2560 mV	L	L	L	L	L	L	L	L	L	H	H	L
512 mV	L	L	L	L	L	L	L	L	L	H	L	H
51.2 mV	L	L	L	L	L	L	L	L	L	H	H	H
25.6 mV	L	L	L	L	L	L	L	L	H	L	H	H
12.8 mV	L	L	L	L	L	L	L	H	L	L	H	H
6.4 mV	L	L	L	L	L	L	H	L	L	L	H	H
3.2 mV	L	L	L	L	L	H	L	L	L	L	H	H
1.6 mV	L	L	L	L	H	L	L	L	L	L	H	H
0.8 mV	L	L	L	H	L	L	L	L	L	L	H	H
0.4 mV	L	L	H	L	L	L	L	L	L	L	H	H
0.2 mV	L	H	L	L	L	L	L	L	L	L	H	H
0.1 mV	H	L	L	L	L	L	L	L	L	L	H	H
0 mV	L	L	L	L	L	L	L	L	L	L	L	L

5.5 Measuring Section

5.5.1 RF Amplifier

5.5.1.1 Checking the Gain

Feed RF signal (level 10 mV, f = 1 to 1000 MHz) to FREQ. METER socket 47 on the front panel and press FREQ. METER key 46. Connect oscilloscope or DC voltmeter to a6 and check level over entire RF range. It must be TTL LOW at all frequencies. When the RF inpu voltage is cut off, the level at a6 must change instantly to TTL HIGH. Subsequently feed RF signal (power 50 mW, f = 1 to 1000 MHz) to the RF input/output socket 48 on the front panel, press TR. key 49 and repeat the measurement.

5.5.1.2 Gain Adjustment

Feed RF signal (10 mV, 100 MHz) to FREQ. METER socket 47 on the front panel and press FREQ. METER key 46. Connect 50-Ω load to ST314 or, in its place, counter Y33. Measure RF output level of the RF amplifier at ST313 using RF insertion unit and 50-Ω termination and adjust to 25 mV by means of R57.

5.5.1.3 Checking and Adjusting Frequency Identification

Feed RF signal (10 mV and f = 520 MHz) to FREQ. METER front panel socket 47 and press FREQ. METER key 46. Connect DC voltmeter or oscilloscope to a4 and increase the frequency of the input signal until the level at a4 changes abruptly from TTL HIGH to TTL LOW. The switching point must be between 530 MHz and 540 MHz. Correct with R87, if necessary.

NOTE: In the case of an overall readjustment or first-time adjustment, the time required can be cut down by preadjusting the DC voltages between MP5 and MP6 to 0 V by means of R87 without applying an RF voltage and then after the RF voltage has been applied adjusting the switching point by carefully turning R87.

5.5.1.4 Checking the Output to the Counter

Feed RF signal (level 10 mV to 1 V, f = 1 MHz to 1000 MHz) to FREQ. METER socket 47 on the front panel and press FREQ. METER 46. Connect 50-Ω load to ST313 or in its place use the mixer board and measure output voltage at ST314 by means of RF insertion unit and 50-Ω termination. It must be about 150 mV over the entire frequency range.

5.5.1.5 Checking the RF Amplifier Without Basic Unit

When measuring the RF amplifier separately, ST312 corresponds to the FREQ. METER input socket 47 and ST311 to the RF input/output socket 48 on the front panel. It should be borne in mind that the signal applied to the RF input/output socket 48 when the RF amplifier is fitted is down 30 dB at ST311. The RF levels directly applied to ST311 must, therefore, be 30 dB less than when checking the RF amplifier with the basic unit.

In addition, when measuring the RF amplifier separately, the respective input (ST312 or ST311) must be selected with TTL level at b7 and the internal RF amplifier gain control be switched on with TTL LOW.

5.5.2 Mixer

5.5.2.1 Checking the IF Output for Input Frequencies < 520 MHz

Feed RF signal (level 35 mV, f = 10 to 520 MHz) to ST322 and LO signal ($f = f_{RF}$ -200 kHz, level 25 mV) to ST321. Apply TTL LOW to a6 and measure level of the 200-kHz IF at a9 using AF voltmeter. It should be about 100 mV.

5.5.2.2 Checking the IF Output for Input Frequencies > 520 MHz

Feed RF signal (level 35 mV, f = 520 to 1000 MHz) to ST322 and LO signal (level 25 mV, $f = 1/2\ f_{RF}$ -100 kHz) to ST321. Apply TTL HIGH to a6 and measure level of the 200-kHz IF at a9 by means of AF voltmeter. It should be about 100 mV.

5.5.2.3 Checking the IF Output with the Circuit Board Fitted

Prior to performing this check, the RF amplifier Y31 and counter Y33 must be adjusted and functioning properly.

Feed RF signal (power 100 mW to 30 W; f = 10 to 520 MHz, with 1-GHz Frequency Extension SMFP-B2 Option fitted: 10 to 1000 MHz) to the RF input/output socket 48 on the front panel and press the TR. 49 and FM 50 keys. Connect AF millivoltmeter to a9 and measure the level of the intermediate frequency (200 kHz ±100 Hz). It should be about 100 mV.

5.5.2.4 Checking and Adjusting the FM Demodulator

The test and adjustment procedures apply to the fitted mixer board. If the circuit board is to be checked separately, set the IF to 200 kHz and apply a TTL H signal to a11.

Feed RF signal (power 100 mW to 30 W; f = approx. 18 MHz; deviation 20 kHz; modulation frequency 1 kHz) to the RF input/output socket 48 on the front panel and press front panel keys 49 TR. and 50 FM. Measure voltage at MP14 by means of AC/DC voltmeter. The DC voltage should be 0 V and the AC voltage 5 V_p corresponding to 3.535 V_{rms} ± 1.5 %. If necessary, the AC voltage can be adjusted by means of R51 and the DC voltage by means of R67.

NOTE: Always make AC voltage adjustment first as it affects the DC voltage adjustment. In the case of major voltage offsets start by making the two adjustments alternatively.

5.5.2.5 Checking the Demodulator Cut-out

Test conditions as in the preceding section.

Measure 0 V DC voltage and 3.535 V_{rms} AC voltage with AC/DC voltmeter at switch B8 pin 4 (switch closed). After cutting off the RF input signal from socket 48 or after pressing the AM key 50 switch B8 must open and no more DC or AC voltage should be measurable.

5.5.2.6 Checking the Deemphasis Filter

The checking procedures apply to the fitted mixer board. If the circuit board is to be checked separately, set the IF to 200 kHz and apply a TTL H signal to a11. The RF signal must be modulated as required.

Feed RF signal (power 100 mW to 30 W, f = about 18 MHz; deviation 5 kHz, modulation frequency 1 kHz) to the RF input/output socket 48 on the front panel and press the front panel keys 49 TR. and 50 φM. Measure AC voltage at b7 by means of AF voltmeter. It should be equal to the voltage at the FM output b6. The permissible offset is ±2%. Vary the modulation frequency of the RF input signal over the range from 300 Hz to 3 kHz and determine the frequency response at the φM output b7. The maximum permissible deviation from the specified frequency response (6 dB/octave) is ±2% relative to the output voltage at the FM output b6 at 1 kHz modulation frequency.

5.5.3 Counter

5.5.3.1 Checking the Count Mode

Control line a10	a9	Selected counter function	Frequency at pin 3 (B1) TTL level
L	L	RF count	f = RF/100 while the counter is enabled
L	H	AF count	f = AF
H	L	Beat count	f = beat frequency
H	H	Off	TTL L

If the lines a9 and a10 are actuated externally and the rest of the instrument functions properly, correct switching of the count modes can be checked at pin 3 (B1).

5.5.3.2 Checking the Reset

At pin 3 (B5) an ECL H pulse of at least 100 ns must be present prior to each count period.

Corresponding TTL H pulses must be present at pins 2 and 14 of B7 and at pins 7 and 15 of B8 and B9.

An inverted TTL pulse must be present at pin 13 (B6).

5.5.3.3 Checking the Clock Inhibit

To check proper functioning of the clock inhibit by means of an oscilloscope, a TTL signal of about 10 MHz must be fed to a13. The ECL signal measured at pin 16 (B5) must have a rise time of better than 10 ns.

$f \gtrless 520$ MHz

Voltages at

a11	14 (B23)	1 (B20)	1 (B21)
TTL L	5.2 V	about -13 V	about +13 V
TTL H	0 V	about +13 V	about -13 V

Adjust the voltage of the 1:4 prescaler B23 at pin 14 to 5.2 V by means of R22.
Prior to this adjustment ensure that a11 is at TTL L level.

5.5.4 AF Amplifier

5.5.4.1 Checking of Input Switching

To perform this check, a properly functioning and at least coarsely adjusted basic unit is required.

Feed amplitude-, phase- or frequency-modulated RF signal within the particular measurement range to the RF input/output socket 48 on the front panel and an AF signal, which is also within the particular measurement range to the AF meter input 31. By pressing one of the keys 11, AM, φM or FM and by pressing key 15, AF level measurement is selected. Connect oscilloscope or AC voltmeter to check whether the particular signal is connected through to the DEMOD. SIGNAL output 37 on the front panel.

The various signals are present at the following AF amplifier inputs:

AF level measurement	5b
FM measurement	6b
φM measurement	7b
AM measurement	8b

Table 5-25

Control signal for input switching:

	Input AF amplifier 5a	6a	Output B20 4	5	6	7	Outputs B22 1	7	9	15
AF level measurement	L	L	H	L	L	L	−15 V	+15 V	−15 V	−15 V
FM measurement	H	L	L	H	L	L	+15 V	−15 V	−15 V	−15 V
φM measurement	L	H	L	L	H	L	−15 V	−15 V	−15 V	+15 V
AM measurement	H	H	L	L	L	H	−15 V	−15 V	+15 V	−15 V

5.5.4.2 Checking the Amplifier Chain

To perform this check, a properly functioning and at least coarsely adjusted basic unit is required.

Successively feed 5.00-V, 500-mV, 50.0-mV and 5.00-mV NF signal to the NF-AC METER socket 31 on the front panel. Press AF level measurement key 15 on the front panel and measure AF level at the output 18b of the AF amplifier by means of AF digital voltmeter. With V_{in} = 5.00 V and V_{in} = 500 mV and f = 50 Hz to 20 kHz it should be 5 V_p corresponding to 3.535 V_{rms} ±2% and with V_{in} = 50.0 mV and V_{in} = 5.00 mV and f = 50 Hz to 10 kHz it should be 5 V_p corresponding to 3.535 V_{rms} ± 3%.

Table 5-26

Control signals for gain setting

Gain	Control line (TTL) 9a	10a	11a
0 dB	L	L	L
20 dB	H	L	L
40 dB	H	H	L
60 dB	H	H	H

5.5.4.3 Checking the Counter Control for AF Ext. Measurement

Feed 10-mV AF signal to NF . AC METER socket 31 on the front panel. Connect oscilloscope to output 12b of the AF amplifier and check signal. It should have TTL format with a duty cycle of about 1:1. Press the AF level measurement key 15 and the AF ext. frequency measurement key 33 on the front panel and check the counter accuracy over the frequency range 20 Hz to 1 MHz. The maximum permissible error is ±1 digit.

5.5.4.4 Adjusting the Counter Control for AF EXT. Measurement

Feed 10-mV AF signal to NF . AC METER socket 31 on the front panel and connect oscilloscope to output 12b of the AF amplifier. Adjust duty cycle of the TTL output signal to about 1:1 by means of R3. Check performance over the frequency range from 20 Hz to 1 MHz.

5.5.4.5 Checking the Counter Control for Beat-frequency Measurement and Frequency Measurement of Demodulated Signal

To perform this check, an adjusted and properly functioning basic unit is required.

Feed frequency- or amplitude-modulated RF signal in the particular measurement range to the RF input/output 48 on the front panel and measure frequency modulation or amplitude modulation, respectively. Press key 36 on the front panel for measuring the frequency of the demodulated signal, connect an oscilloscope to output 13b of the AF amplifier and check the output voltage for TTL format (squarewave).

Feed unmodulated RF signal in the given frequency and power range to the RF input/output 48 on the front panel, press TR. key 49 and offset the frequency of the RF synthesizer by 5 Hz to 10 kHz from the frequency of the signal fed in (keyboard 25 and variation keys 2). Press key 35 for beat-frequency measurement, connect an oscilloscope to output 13b of the AF amplifier and check the output voltage for TTL format (squarewave).

In both measurements, the frequency of the output signal of 13b (frequency of the demodulated signal or beat frequency) is read out on the AF display 13 on the front panel.

5.5.5 DC Amplifier

5.5.5.1 Checking the Control Functions for Current, Voltage and Power Measurement

Table 5-27

TTL level at the control lines a13	a12	Function selected	Relevant input, Input signal	Relevant output	Transmission function
L	L	Power	a9, a10 DC with AC	b11	DC component with V approx. 1
		Mod. depth		b8	AC component approx. $V_{AC} \times \frac{5\ V}{V_{DC}}$
L	H	Voltage	a7, a8 DC	b11	V = 1/3
H	L	I low: readout measurement value I high: sample measurement value	a17, a18 a17, a18 DC	b11	V = 1 *)
H	H	I high: readout measurement value I low: sample measurement value	a6, a5 DC	b11	V = 1 *)

*) The current is measured by constantly changing over between these two switching states.

5.5.5.2 Checking the Control Functions for the Detectors

Table 5-28

Log. level at control lines b12 b13 b7	Function selected	Input / Output	Transmission function
L L	None	a4	
L H L	Pos. peak-value measurement		V_{b9} (DC) = 2 x pos. input amplitude
L H H	Neg. peak-value measurement	/	V_{b9} (DC) = 2 x neg. input amplitude
H L	Rms-value measurement	b9	V_{b9} (DC) = 2.82 x input rms voltage, approx.

5.5.5.3 Adjusting the True rms Rectifier

a) Connect digital voltmeter to b9.

b) Switch on true rms meter (b12 at H level)

- Offset adjustment:

c) Take a4 to 0 V.

d) Adjust R51 and R52 for 0 V at the output.

- Gain adjustment:

e) Connect link for signal through-connection.
Apply 3.54 V_{rms} or 0.354 V_{rms} to input 4a.

f) Adjust R53 for 10 V DC or 1 V DC, respectively.
With the aid of R52, both voltages can be correctly adjusted at the same time.

5.5.5.4 Adjusting the Offset and Common Mode of the Current, Voltage and Power Section

B1: - Connect digital voltmeter to MP1.
- Short-circuit 5a and 6a.
- Adjust R3 for 0 V ±0.1 mV.
- Apply common-mode 30-V input voltage to 5a, 6a.
- Adjust R7 for 0 V +0.1 mV (with relay open and closed)

B2: - Adjust B2 analogously (see B1).

B3: - Connect digital voltmeter to MP3.
- Short-circuit 7a and 8a.
- Adjust R18 for 0 V ±0.1 mV.

B4, B5:
- Connect digital voltmeter to pin 6 (B4).
- Short-circuit a9 and a10.
- Adjust R23 for 0 V ±0.1 mV.
- Connect digital voltmeter to pin 6 (B5).
- Adjust R32 for 0 V ±0.1 mV.

5.5.5.5 Adjusting the RF Power Measurement

The following adjustments of the functional group RF power measurement and modulation-depth measurement are made in conjunction with the RF distributor.

-Distortion compensation

a) Program power measurement function at a13, a12 (apply 0.0).
b) Feed RF signal (10 MHz, 100 mW, 80% AM, modulation frequency 1 kHz) to RF input 48 on the front panel.
c) Connect distortion meter to b8.
d) Adjust R72 for minimum distortion.

-Adjustment of power indication

In order to achieve the measurement accuracy guaranteed in the data sheet, it may be necessary to fit the coaxial 50-Ω resistor, which is supplied with the instrument, to rear socket 54.

e) Feed RF signal (10 MHz, 2 W, unmodulated) to RF input 48 on the front panel.
f) Connect digital DC voltmeter to b10.
g) Adjust R70 for 1.280 V.
h) If necessary, repeat steps c) and d).
i) 19b at TTL H: Modulation-depth and power measurement interrupted.

The following adjustments must be made after the instrument has been assembled and the A/D converter and the true rms meter have been adjusted because they are to be observed on the displays of the instrument.

5.5.5.6 Adjusting the Modulation-depth Indication

- High power

  a) Feed RF signal (2 W, 50% AM, modulation frequency 1 kHz) to RF input 48 on the front panel.

  b) Press TR. key 49.

  c) Adjust R43 for correct modulation-depth indication.

- Low power

  d) Feed RF signal (100 mW, 50% AM, modulation frequency 1 kHz) to RF input 48 on the front panel.

  e) Adjust R36 for correct indication.

  f) Check settings a), b), c).

5.5.6 Filters

5.5.6.1 Checking the CCITT Filter

The reference attenuation values of the CCITT filter are listed in the Table 5-29. It should be borne in mind that the distortion of the signal generator and its hum voltage at low frequencies may cause erroneous measurements. A bandpass filter should, therefore, be connected between the signal generator and the CCITT filter.

Table 5-29

Frequency Hz	$20 \log \frac{V_f}{V_{fo}}$ dB	Permissible deviation dB
Frequency/Hz	Attenuation/dB	Tolerance/dB
50 100 150 200	-63.0 -41.0 -29.0 -21.0	±2
300 400 500 600	-10.6 -6.3 -3.6 -2.0	±1
800	0.0	±0
1000 1200 1500 2000 2500 3000	+1.0 0.0 -1.3 -3.0 -4.2 -5.6	±1
3500	-8.5	±2
4000 5000	-15.0 -36.0	±3
6000 > 6000	< -43.0 < -43.0	- -

The passband attenuation is adjusted at 800 Hz using R4.
The performance of the notch filter can be checked against Fig. 4-17.
The through-line section is not adjusted.

5.5.6.2 Adjusting the Notch Filter

To adjust the notch filter, first set all potentiometers to their midposition and then adjust the 1000-Hz notch.

Apply a distortion-free signal of exactly 1000 Hz and about 1 V_{rms} to the input using the AF generator and the octave filter. Insert link and connect probe of a sensitive oscilloscope to BR80. By alternately turning R66 and R68 adjust for minimum.

Apply signal of same input voltage and 1010 Hz and with the link inserted adjust for minimum at BR95 using R97. Subsequently adjust potentiometer R117 for minimum at B110 pin 6 at 990 Hz.

Similarly, adjust the 300-Hz notch at the frequencies 300 Hz, 303 Hz and 297 Hz using the potentiometers R72, R73, R96 and R116 and the 500-Hz notch at the frequencies 500 Hz, 505 Hz and 495 Hz using the potentiometers R17, R18, R30 and R50.

5.5.7 A/D Converter

5.5.7.1 Checking the Switch Control Signals for Modulation Processing

Table 5-30

Programmed modulation function Int.	Ext.	Logic levels at contact 2, 33 of B10 / corresponding to bus line 4a (LSB)	B12 / 5a	B13 / 6a	B14 / 7a	B15 / 4b	Signal flow
AM	None	H	L	L	L	L	8b ⟶ 17a
AM	FM	H	H	H	L	L	8b ⟶ 17a and 19b ⟶ 18a
AM	φM	H	H	L	L	L	8b ⟶ 17a and 19b - filter ⟶ 18a
FM	None	H	L	L	L	L	8b ⟶ 17a
FM	AM	H	H	H	L	L	8b ⟶ 17a and 19b ⟶ 18a
φM	None	L	L	L	H	L	8b - filter ⟶ 17a
φM	AM	L	L	H	H	L	8b - filter ⟶ 17a and 19b ⟶ 18a
None	AM	H	L	L	H	H	19b ⟶ 18a
None	FM	H	L	L	H	H	19b ⟶ 18a
None	φM	H	L	L	H	L	19b - filter ⟶ 18a

5.5.7.2 Checking the Frequency Response of the Preemphasis Filter

Enter modulation function: "Int. φM" and check frequency response of the filter between 8b and 17a against the following table:

Frequency	Attenuation (dB)	Tolerance (dB)
100 Hz	40	±0.1
1000 Hz	20	±0.1
6000 Hz	4.44	±0.1
10000 Hz	0	±1
> 10000 Hz	> 0	

5.5.7.3 Checking the DC Amplifier

- Apply 100 mV_{DC} to 11b and measure at 10b.
  Check gain between 11b and 10b against the following table.

Table 5-31

TTL Levels at 12b	9b	13b	13a	Gain
L	X	X	X	11b separated from 10b
H	L	L	L	0 dB
H	H	L	L	10 dB
H	L	L	H	20 dB
H	H	L	H	30 dB
H	H	H	H	40 dB

5.5.7.4 Checking the A/D Converter B6 and the Tri-state Drivers B7, B8 and B9

Apply voltages to BR2 in accordance with Table 5-33. Apply TTL H level to line a8 (initiative conversion) and check the logic levels present at the data bus.

Table 5-32

Input signals: Voltage at BR2	Input signals: TTL levels at 12a	11a	Output signals: TTL levels at 7b	6b	5b	4b	7a	6a	5a	4a
0 mV	H	L	X	X	X	X	X	X	L	L
0 mV	L	H	L	L	L	L	L	L	L	L
10 mV	L	H	L	L	L	L	L	L	L	H
20 mV	L	H	L	L	L	L	L	L	H	L
40 mV	L	H	L	L	L	L	L	H	L	L
80 mV	L	H	L	L	L	L	H	L	L	L
160 mV	L	H	L	L	L	H	L	L	L	L
320 mV	L	H	L	L	H	L	L	L	L	L
640 mV	L	H	L	H	L	L	L	L	L	L
1280 mV	L	H	H	L	L	L	L	L	L	L
2560 mV	H	L	L	L	L	L	L	L	L	H
5120 mV	H	L	L	L	L	L	L	L	H	L

5.5.7.5 Adjusting the A/D Converter

The A/D converter board has two separate ground lines. Only one of them is to be used as ground reference for all adjustments, and connections can be made to this either at the ground terminal of BR1 or BR2, or at the ground terminal brought out to the DC amplifier.

DC amplifier adjustment

- Connect BR1 to ground terminal.
- Connect digital voltmeter to BR1.
- Enter 40 dB gain (apply TTL H level to 9b, 13a, 13b).
- Adjust R12 for 0 V ±1 mV.
- Connect digital voltmeter to contact 6 (B5).
- Adjust R18 for 0 V ±1 mV.

Adjustment of A/D converter B6

- Apply TTL H level to initiative conversion line.
- Connect BR2 to ground terminal.
- Adjust R35 so that pins 3 to 11 (B6) are at TTL L level and pin 12 (B6) just changes from TTL H to TTL L level (do not turn any further).
- Apply 10.22 V to BR2.
- Adjust R30 so that pins 3 to 11 (B6) are at TTL H level and pin 12 (B6) is at TTL L level.

  The modulation processing circuit does not require adjustment.

5.5.7.6 Checking and Adjusting the Programmable Attenuator

- Checking the control function:

  Apply 1024 mV at BR1 and measure the output voltage of the programmable attenuator at MP1. It is: 10-bit dual number at pin 4 (LSB) to pin 13 (MSB) of B3 in mV (0 = TTL Low / 1 = TTL High).

- Offset adjustment:

  Plug BR1 on ⊥, apply TTL High level at pin 4 to pin 13 of B3 and adjust with R8 for 0 V ±2 mV at MP1.

5.5.7.7 Checking the Input Switching

Logic level at B13 pins 2,3	Test condition	Signal flow
0	TTL Low at pins 4 to 13 of B3	b17 ⟶ MP2 b8 interrupted
1		b17 interrupted b8 ⟶ MP2

5.5.8 Voltage Supply

5.5.8.1 Performance Check - Power Transformer and Rectifier

(See circuit diagram 332.015 B1.4)

Connect either the DC-DC converter or a dummy load of about 90 W to the power (mains) transformer. At 220 V or 110 V AC supply voltage (depending on the position of the voltage selector on the rear panel), a secondary voltage of about 16 to 17 V_{rms} is measured and after the bridge rectifier GL102-105 a DC voltage of about 22 V with a superimposed signal of double the AC supply frequency < 1 V_{pp} is measured at C101.

5.5.8.2 Checking the DC-DC Converter

To check the performance of the DC-DC converter, measure the voltage at various test points.

MP1: +5 V DC

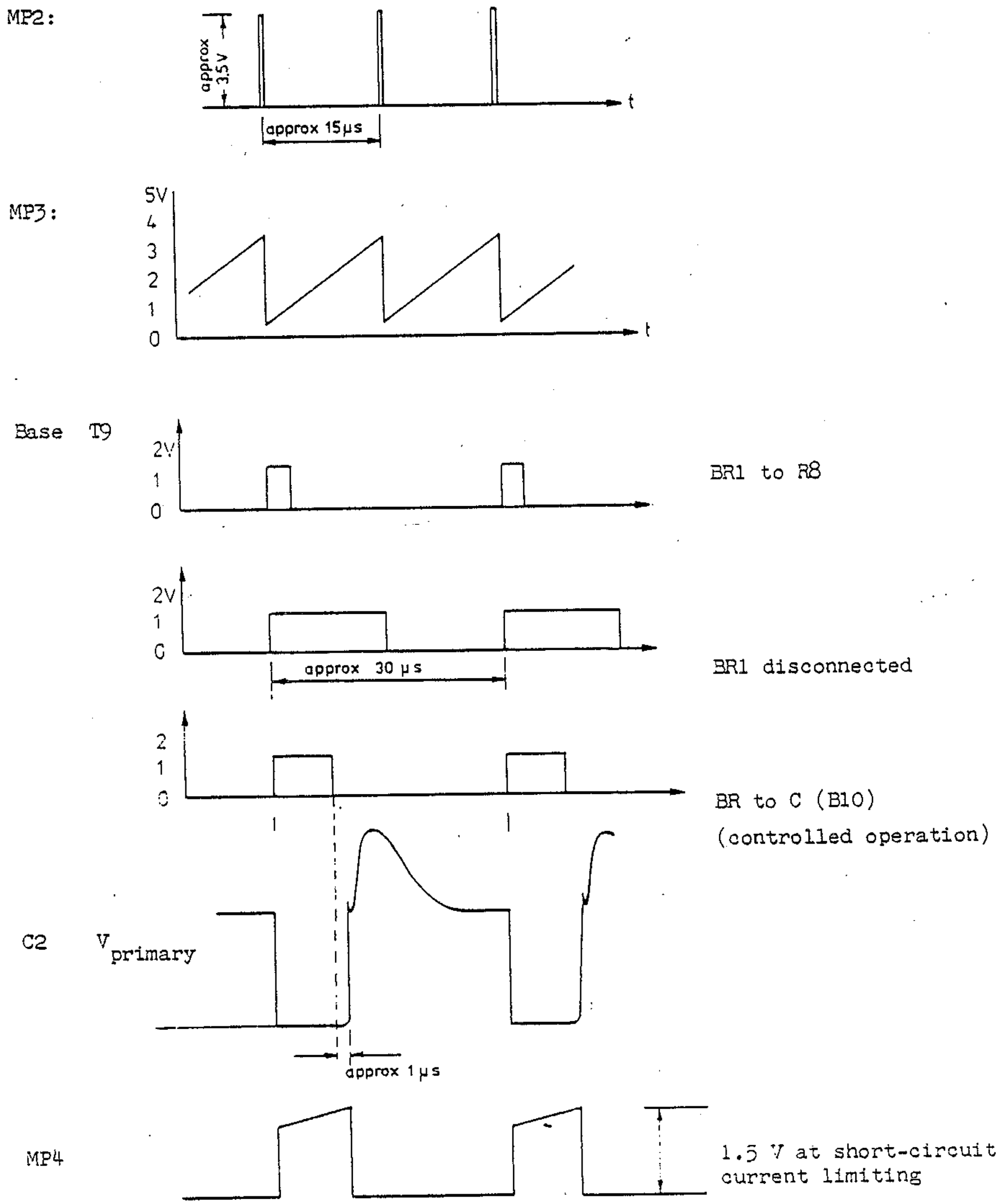
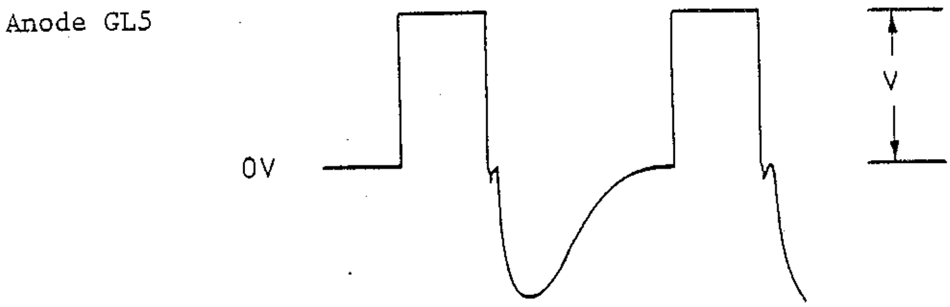
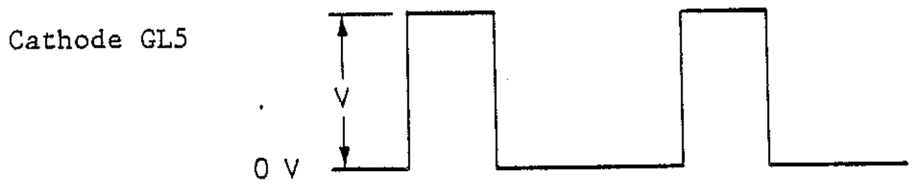


Fig. 5-1 Primary voltage characteristics of the DC-DC converter

The voltages on the primary are almost the same for all four converters.





V = about 1 x V primary at +5 V
about 4 x V primary at +15 V (in phase opposition at -15 V)
about 6 x V primary at +20 V

Fig. 5-2 Secondary voltage characteristics of the DC-DC converter

5.5.8.2.1 Adjusting the Switching-mode Converter

It is recommended that a check of the primary voltage conditions be carried out before putting the instrument into operation to avoid damage to components in case of fault.

To check the primary voltages, connect the board without the power section to the primary voltages and check the voltage against section 5.5.8.2 by means of an oscilloscope.

Then put instrument into operation with the power section.

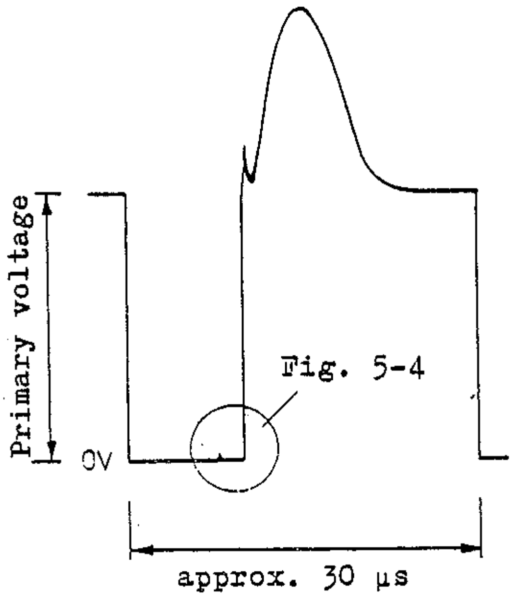
Preparations:

- Connect variable dummy loads with ammeters to all voltages and adjust low load (about 1/3 of full load).
- Insert only 5-V IC. Remove all other control ICs.
- Remove all synchronizing links (BR32, 62, 92, 102).
- Connect BR1 to C (B10) (close control loop).

NOTE: The converter must not be operated with a high load connected for an extended period of time when it is not adjusted.

Adjustment of switching transistor:

- Connect oscilloscope between C2 and primary ground.
- Short-circuit potentiometer R6 (turn fully clockwise).
- Switch on.
- Slowly increase load until full load is reached (5 A).
- Turn R6 counterclockwise until the switching transistor is operating just at the saturation level.
- Increase load until short circuit occurs.
- Check whether the saturation level is still just reached in the case of an overload.



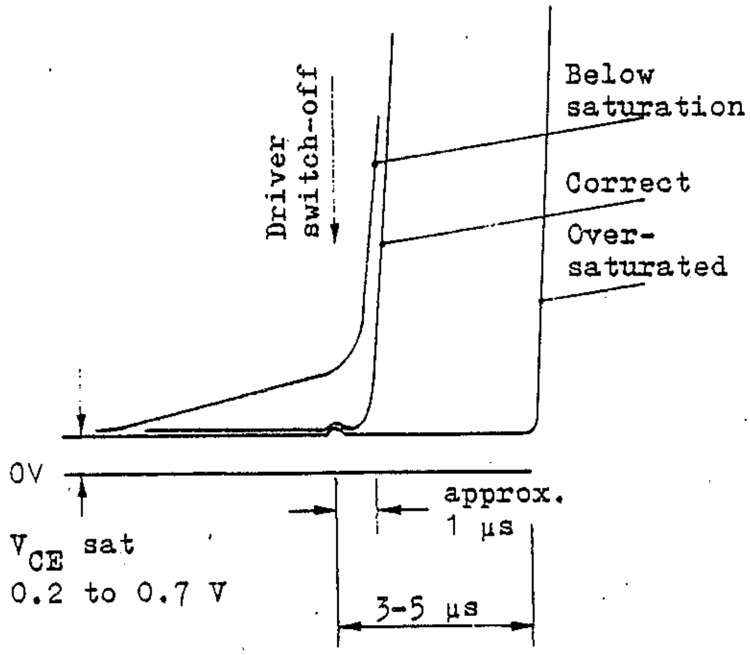


Fig. 5-3 Collector voltage

Fig. 5-4 Collector voltage

T10, 11 must be operated just at saturation level, not at oversaturation because of the dissipation in the driver and the long switching times but also not below saturation because of the dissipation in the switching transistor proper.

NOTE: Repeat the adjustment of the switching transistor if another power section is assigned to the DC-DC converter or if a transistor is replaced in the power section.

Adjust the output voltage by means of R20.

Switch on all the other voltages.
This is done in the same way as for the +5-V supply. The other switching mode converters can be operated independent of one another and the 5-V converter without the synchronizing links BR32, 62, 92 being connected.
Their switching frequencies are then somewhat below the switching frequency of the 5-V converter. After connecting the synchronizing links, these frequencies are locked to that of the 5-V converter. The 5-V and 20-V supplies must be operating before switching on the 32-V supply. The 32-V supply cannot be adjusted. For switching on the following sequence must be observed:
+5 V, +15 V, -15 V, +20 V, +32 V.

5.5.8.3 Overvoltage Protection for Supply Voltages

The overvoltage protection circuit protects the instrument if one of the supply voltages is inadmissibly high. The signal indicating that an overvoltage exists, is produced on the regulator board. This current controls one of the two optoisolators B111 or B112 which in turn fires the thyristor GL112 almost short circuiting the secondary of the power transformer (primary voltage of the DC-DC converter). As a result, the power fuse blows.

This performance check is not done with the board in the instrument.
The above function is simulated.

5.5.8.4 Checking the Regulator

(Circuit diagram 332.2918)

For the performance check, the input voltages +5 V (at 1ab), +15 V (16ab) and +32 V (5ab), -15 V (14ab), +20 V (18ab) must be applied to the regulator board.

The -5.2-V voltage produced on the board is measured at 3ab. The permissible tolerance is ±0.1 V. The 28-V voltage is measured at 20ab. The tolerance is ±0.1 V.

If all of the six voltages required in the instrument are present, the six LEDs GL20, 32, 50, 52, 54 and 56 light up.

Apply an AF signal of about 10 mV and a frequency in the audio range to pin 7a and 6a. Check the function of B1 at 8b. The gain should be about 47. Check the function of B10 at 9b. The gain should be about 50.

Check the overvoltage protection response with the board removed.

For this purpose, connect an ammeter to 11a and increase the -15-V voltage to -17 V. At -15 V, the ammeter does not give a reading. Between -15.2 and 17 A, a current of about -5 mA commences to flow.

Similarly a current starts to flow at 13a if one of the positive voltages is increased accordingly.

5.5.8.5 Performance Check - Battery Input

Apply a DC voltage to the battery sockets on the rear panel and switch on instrument. If the polarity of the battery connection is correct, the instrument will operate at DC voltages between 11 and 33 V. DC voltages > 33 V must not be applied. The power supply is protected against reverse polarity.

5.5.9 Checking and Adjusting the Adjacent-channel Power Meter Option SMFP B61

5.5.9.1 Functions of Control Lines

TTL control signals at 7b	6b	5b	Setting of gain/attenuation between ST2 and C17
L	L	L	-40 dB
L	L	H	-30 dB
L	H	L	-20 dB
L	H	H	-10 dB
H	L	L	0 dB
H	L	H	+10 dB
H	H	L	+20 dB
H	H	H	+30 dB

TTL control signals at 9b	8b	The following IF filter is connected into signal path:
L	L	no filter
L	H	B1 (±8 kHz)
H	L	B2 (±4 kHz)

TTL control
signals at

10b	
L	Calibration: signal path ST341/342 to B12 7-4 MP1
H	Measurement: signal path ST9a B12 6-4 MP1

TTL control
signals at

5a	
L	Open level control loop Hold control voltage at 4a
H	Close level control loop

6a	
L	Disconnect measured value (MP11)
H	Connect measured value through to 12B (A/D converter input)

5.5.9.2 Function Check of Signal Path

- Low-pass filter with 650 kHz cut-off frequency between ST341/342 and MP1:
  If 50 mV into 50 Ω is present at ST341/342, the voltage present at MP1 should be 25 mV in the pass band of the filter.
- Tuned amplifier with about 34 dB gain at 455 kHz, circuit Q about 7 between MP1 and ST1:
  If 50 mV is present at MP1, approximately 2.5 V should be present at ST1.
- Ceramic filter B1 (455 kHz, ±8 kHz bandwidth, 7 to 10 dB insertion loss)
- Ceramic filter B2 (455 kHz, ±8 kHz bandwidth, 8 to 12 dB insertion loss)

  Between ST1 and ST2:
  If 2.5 V is present at ST1, about 1 V should be present at ST2.
- Switchable amplifier/attenuator between ST2 and ST3:
  Dynamic range at input: 100 μV to 1 V with 455 kHz;
  Dynamic range at output: up to 15 mV, max.
- Rms detector circuit between ST3 and MP10
  Transmission characteristics: DC output voltage at MP10 is proportional to the square of the rms input voltage at ST3.
  Overdrive capacity at input: about 15 mV.

- Low-pass filter with about 150 Hz cut-off frequency between MP10 and MP11
  Gain 2

- Integrator between MP10 and 4a
  Integration time constant 1/3 s

5.5.9.3 Adjusting the Adjacent-channel Power Meter Option

The adjustments under 1) or 2) are carried out on the board alone, without the basic unit. The adjustment under 3) is carried out in conjunction with the basic unit.

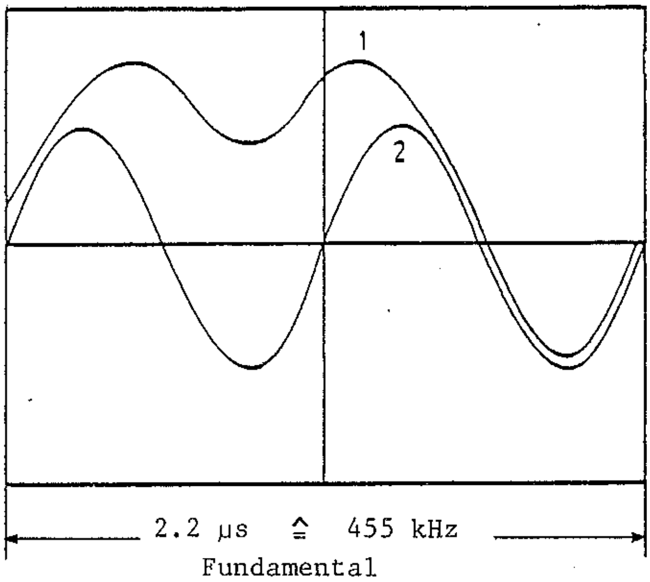
1) Adjusting the input amplifier
   Feed 10-mV, 455-kHz sinewave signal into ST9a. Disconnect link from ST1 and connect oscilloscope probe to ST1,1. Vary the capacitance of C4 until resonance is obtained at 455 kHz ±3 kHz.

   The gain at resonance is about 20 dB.

   NOTE: Since the screening cover influences the resonant frequency, the (top) cover should be on when adjusting for maximum resonance.

2) Adjusting the rms-value meter
   - Adjustment of offset:
     Connect voltmeter to MP10.
     Connect link at ST3 to ground.
     Vary R41 until 0 V ±5 mV is present at MP10.

   - Adjustment of balance
     Apply 455-kHz signal of about 10 mV into ST3 (connect link so that it will allow the signal to pass).
     Remove C32. Connect oscilloscope probe to MP8 or MP9. Adjust R39 until the following oscillograms are obtained at MP8 and MP9, respectively.



Replace C32
Check adjustment of offset
Check adjustment of balance

1 = not adjusted
2 = adjusted

3) Adjustment of the level control loop

The level control loop of the Adjacent-channel Power Meter Option (slow RF amplifier control) is activated when 10b is at TTL H.

Feed two signals spaced about 1.25 kHz apart into the RF input 48 or 47 (e.g. combine 159.999 375 and 160.000 625 MHz at DVS).

Connect oscilloscope to MP1.
Alternately cut in 10 kHz channel spacing (B95 with 8 kHz bandwidth in the signal path) and 20 kHz channel spacing (B90 with 15 kHz bandwidth in the signal path).

Adjustment using R57:
The measured signal f ≈ 455 kHz has an envelope with a frequency of 1.25 kHz (sinusoidal). The envelope must on the one hand show now distortion and on the other hand be as large as possible (70 to 80 mV peak).

5.5.9.4 Interface Data

ST B41/42	50 mV into 50 Ω if the level fine adjustment is on 0 dB, 0.4 to 520 MHz	
9a	IF 455 kHz approx. 50 mV	
8b, 9b, 10b	TTL level	
5b, 6b, 7b, 6a, 5a	TTL level	
12b	Measured value 0 to 10 V DC voltage	
4a	Control voltage: typical 7 V RF level too low: 10 V RF level too high: 0 V	Voltages with level control loop closed dependent on response of RF amplifier
1a,b	+5 V approx. 1 mA	
2a,b	⊥	
14a,b	-15 V approx. 50 mA	
15a,b	⊥	
16a,b	+15 V approx. 50 mA	

5.5.10 Troubleshooting - RF Millivoltmeter Option SMFS 2B8

This section covers all measurements, measurement values and settings required for checking the performance of the individual stages of the set and for troubleshooting and repair, if necessary.

5.5.10.1 Chopper Generator

A symmetrical AC squarewave voltage of a frequency of about 23 Hz and an amplitude of

$$V_{pp} \approx 12\ V$$

is available at the outputs of generator B40. The negative component of the generator voltage switches the chopper transistors T1 and T2.
The synchronous detector B11 is controlled directly from the generator voltage.

5.5.10.2 Reference Generator

Generator B30 supplies a symmetrical AC squarewave voltage of a frequency of 5 kHz and an amplitude of +15 V for the reference generator. The frequency of this generator can be varied slightly by means of R30. The DC output voltage of the reference generator is transformed into an AC squarewave voltage of equal amplitude in the B25 from where it is applied to the transformer TR2 via the resistors R22 to R24. The transformer TR2 together with C7 forms a damped 5-kHz resonant circuit. Thus a sinewave voltage is obtained from the AC squarewave voltage, which is boosted in the driver amplifier B10 and supplied to the comparison detector in the measuring head. The DC input voltage of the reference generator is available at the test socket BU3, pin 13. The 5-kHz AC output voltage is available at socket BU3, pin 5. If the DC input voltage at BU3.13 is 1 V the AC output voltage of the reference generator at BU3.5 must be about 300 mV (NOTE: output impedance at the test socket BU3.5 = 10 kΩ).

5.5.10.3 Adjustment

Prior to making any adjustments on the RF Millivoltmeter Option check that the DC meter of the basic unit is functioning properly.

The ambient temperature should be between 20 and 25°C. A warm-up period of at least 10 min must be allowed for.

It is best to use the probe together with the BNC adapter (insertion adapter) as measuring head. An insertion unit may also be used but in this case a T piece must be connected ahead of it to gain access to the inner conductor for voltage measurements.

Adjustment procedure:

- Apply a signal of 1 Hz and V_{rms} = 1 V to the measuring head.

Resonance adjustment:

- Adjust R30 until the display on 5 is exactly at minimum.

Chopper adjustment:

- Interrupt test voltage supply and set R38 to its right-hand stop.
- Measure the voltage at BU3.14 with an oscilloscope and adjust the AC component (approx. 22 Hz) to minimum using R45.

Offset adjustment:

- Adjust R38 so that the display on 5 fluctuates between 0 and 0.3 mV (no voltage may be present at the measuring head).

Gain adjustment:

- Feed to measuring head voltage of 1 Hz, V_{rms} = 1 V ±1 mV and distortion factor < 0.3%.
- Adjust R21 until an RF voltage of 1.000 V ±1 mV is displayed on 5.

Fine adjustment for low RF voltages:

- Feed in AC voltage (1 MHz, 1.2 mV ±1%).
- Adjust R98 until 1.2 mV is displayed on 5.

5.5.10.4 Replacing the Probe Diodes

(See Fig. 9 in the appendix)

If any of the diodes in the probe have been destroyed by an excessively high input voltage, all four diodes must be replaced. A selected quad can be ordered from R&S under the order number 243.9001. For replacement proceed as follows:

a) Push the cable bushing back.

b) Remove the retaining screw from the probe sleeve.

c) Pull off the probe sleeve in the direction of the cable.

d) Replace the quad GL1I to GL1IV shown in Fig. 9 with the aid of tweezers.

!!! Do not solder, diodes are plugged in !!!

Should any soldering be required on the probe, first remove the four diodes from their sockets in order not to expose them to excessively high temperatures.

5.5.10.5 Replacing the Diodes in the 10-V and 100-V Insertion Units

(See Fig. 10 in the appendix)

If any of the diodes in the insertion units have been destroyed by an excessively high input voltage, all four diodes must be replaced. A selected quad can be ordered from R&S under the order number 288.8304.
For replacement proceed as follows:

- Unscrew engraved cover. Now all four diodes are accessible.
- Pull out the diodes GL1III and GL1IV towards the top.
  The leads rest in miniature sockets; they are not soldered.
- The diodes GL1I and GL1II are also plugged in. First pull out the lead facing the coaxial section. Then pull the diode towards the front thus unplugging the other lead from the miniature socket provided in the partition wall of the compartment.
- The location of the new diodes can be seen from Fig. 10.

ROHDE&SCHWARZ
MÜNCHEN

Bilder
Figures

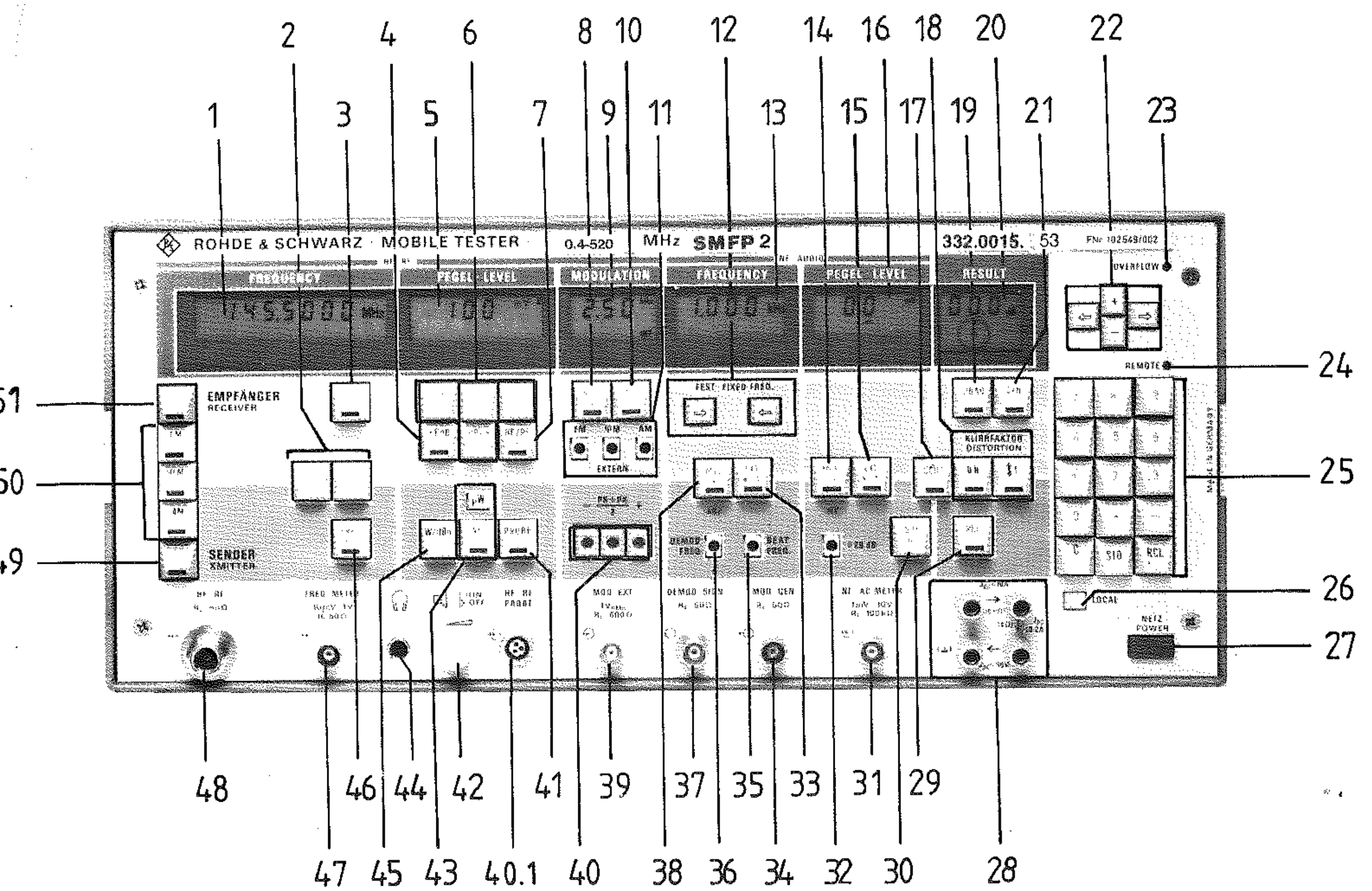


Bild 2-3 Frontansicht
Fig 2-3 Front panel

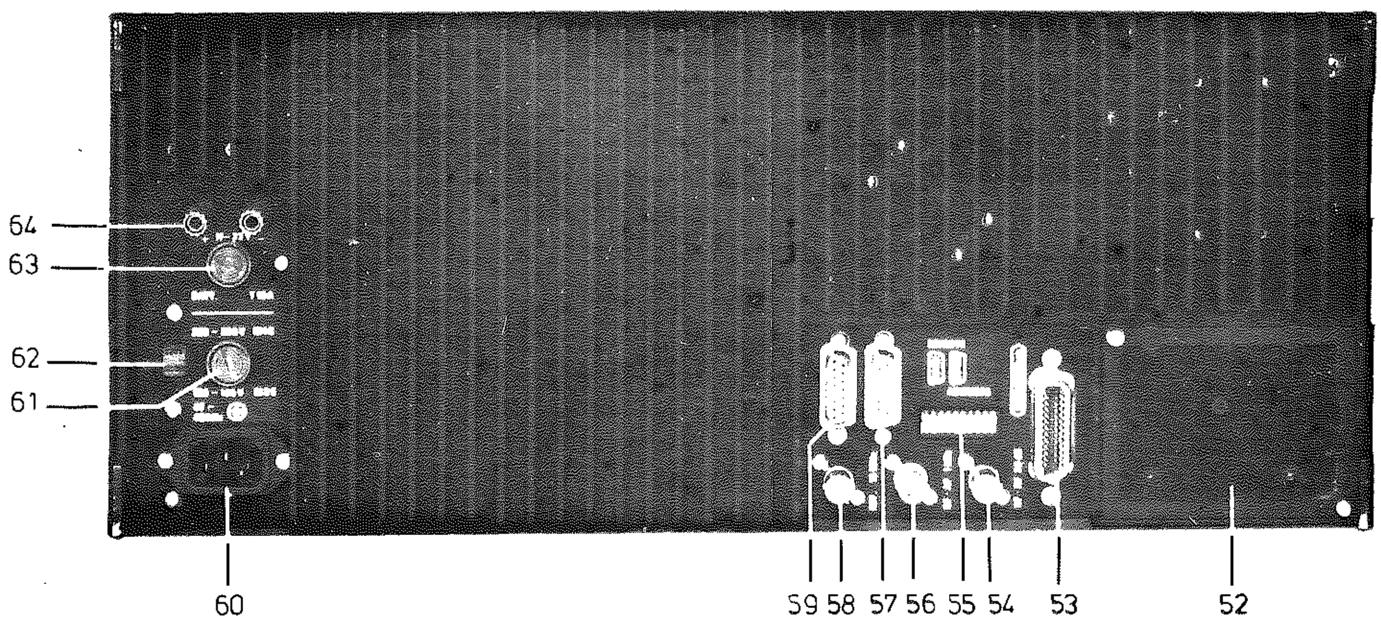


Bild 2-4 Rückansicht
Fig 2-4 Rear panel

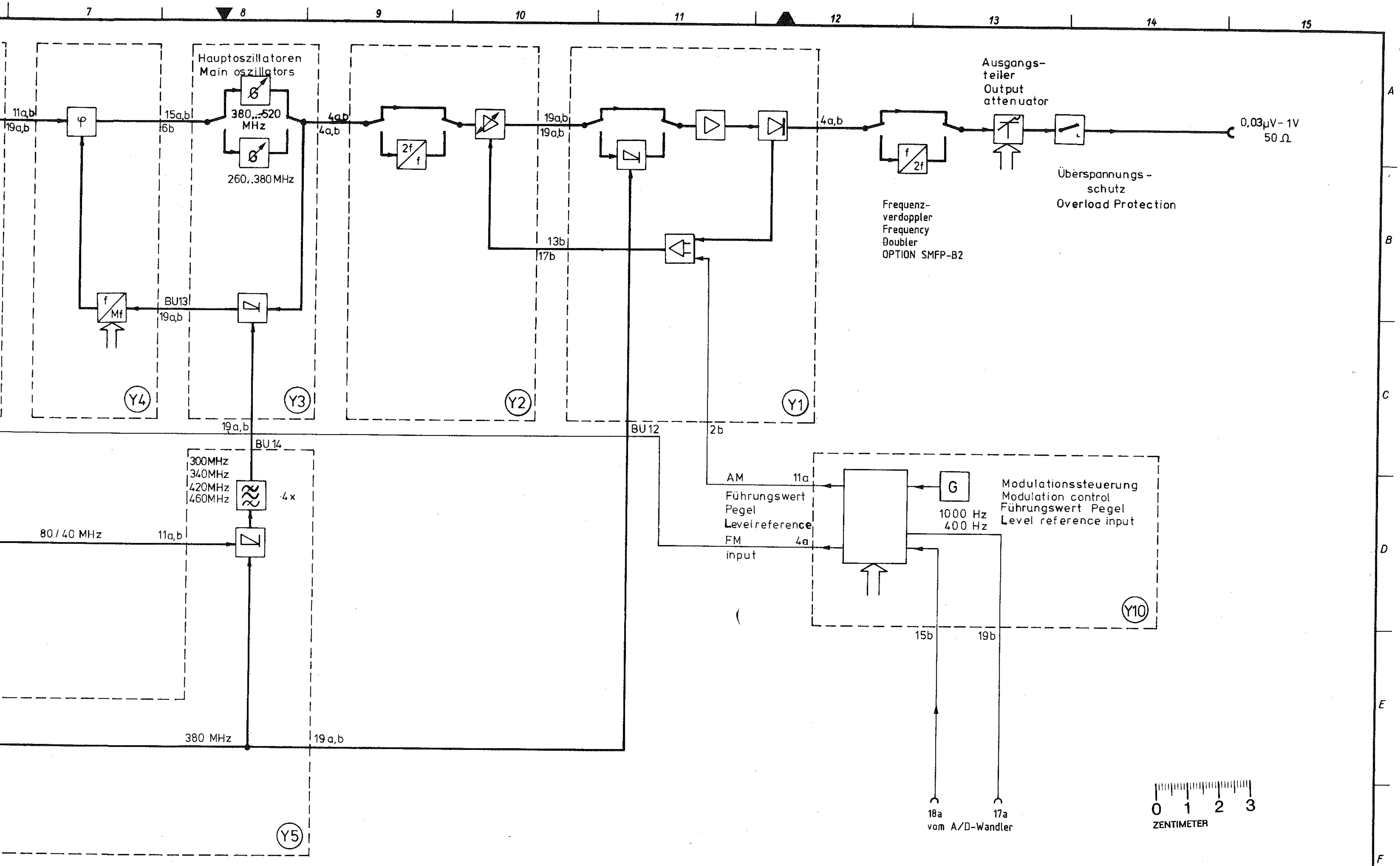
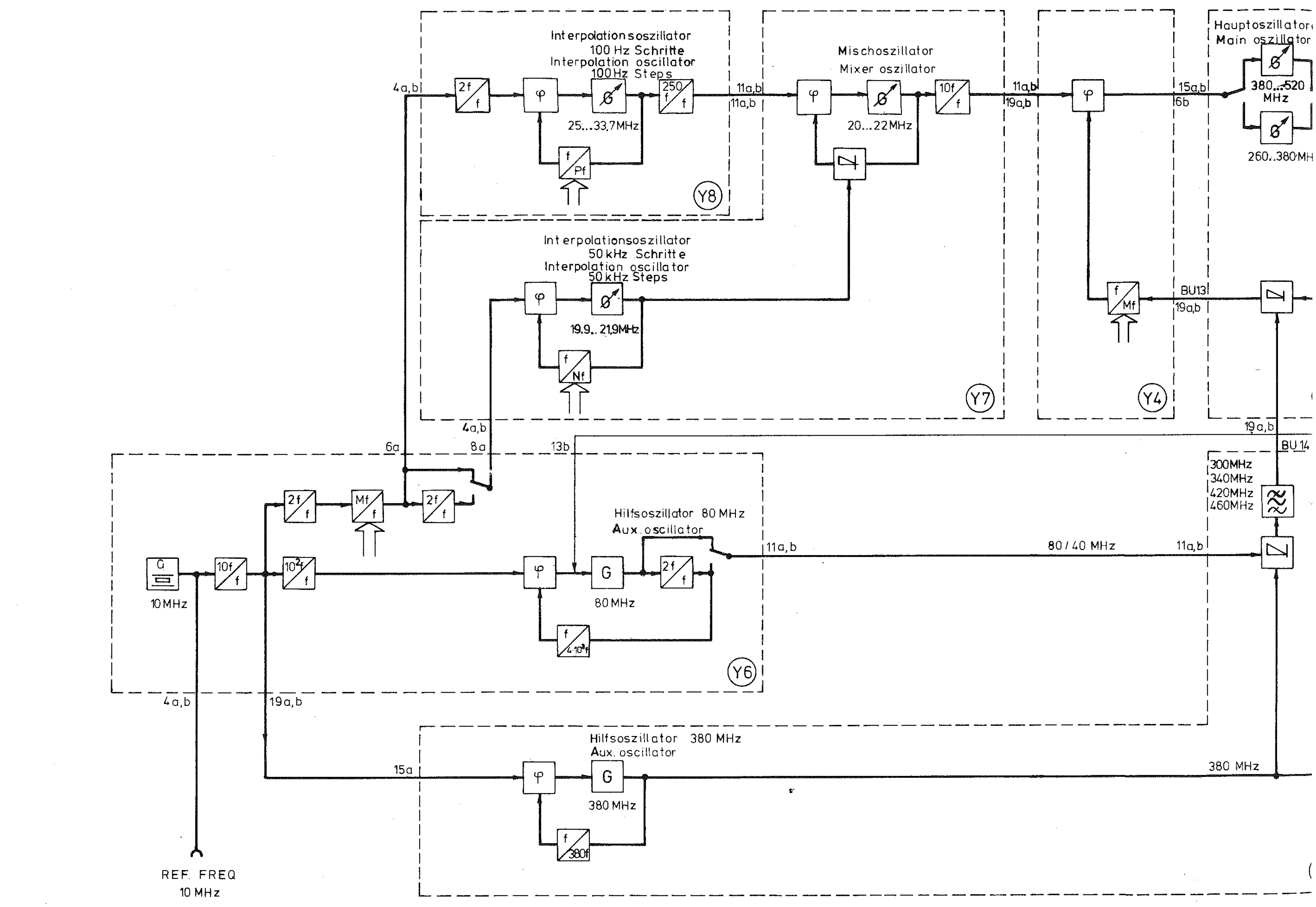


Bild 4-25 HF-Generator
Fig. 4-25 HF generator



Diese Zeichnung ist unser Eigentum. Vervielfältigung, unbefugte Verwertung, Mitteilung an andere ist strafbar und schadenersatzpflichtig.

ROHDE & SCHWARZ · MÜNCHEN

Änd.-zust.	Änd. Mittlg. Nr.	Datum	Name

Zeichn.-Nr. 346.2250 - 4.65

PF 095.4115

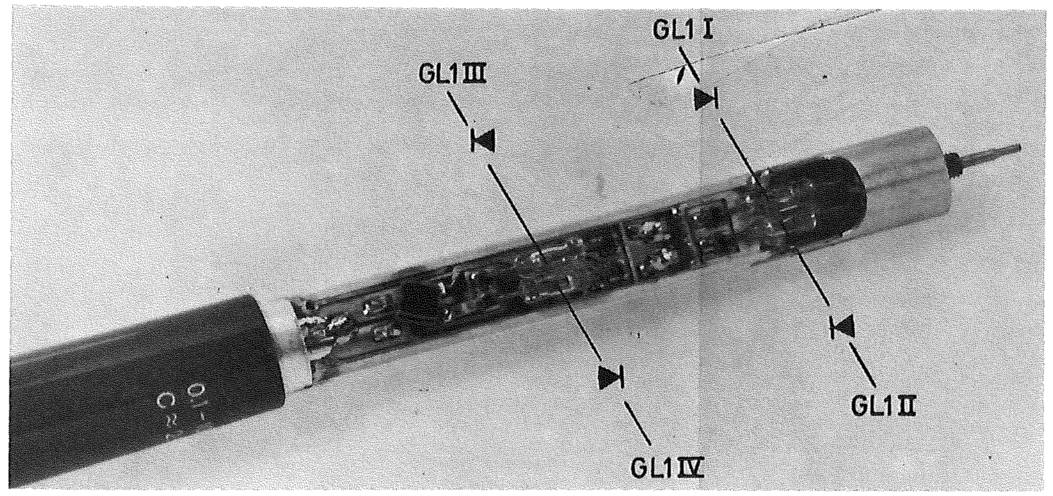


Bild 9 HF-Tastkopf; Lage der Dioden

Fig. 9 RF probe; location of diodes

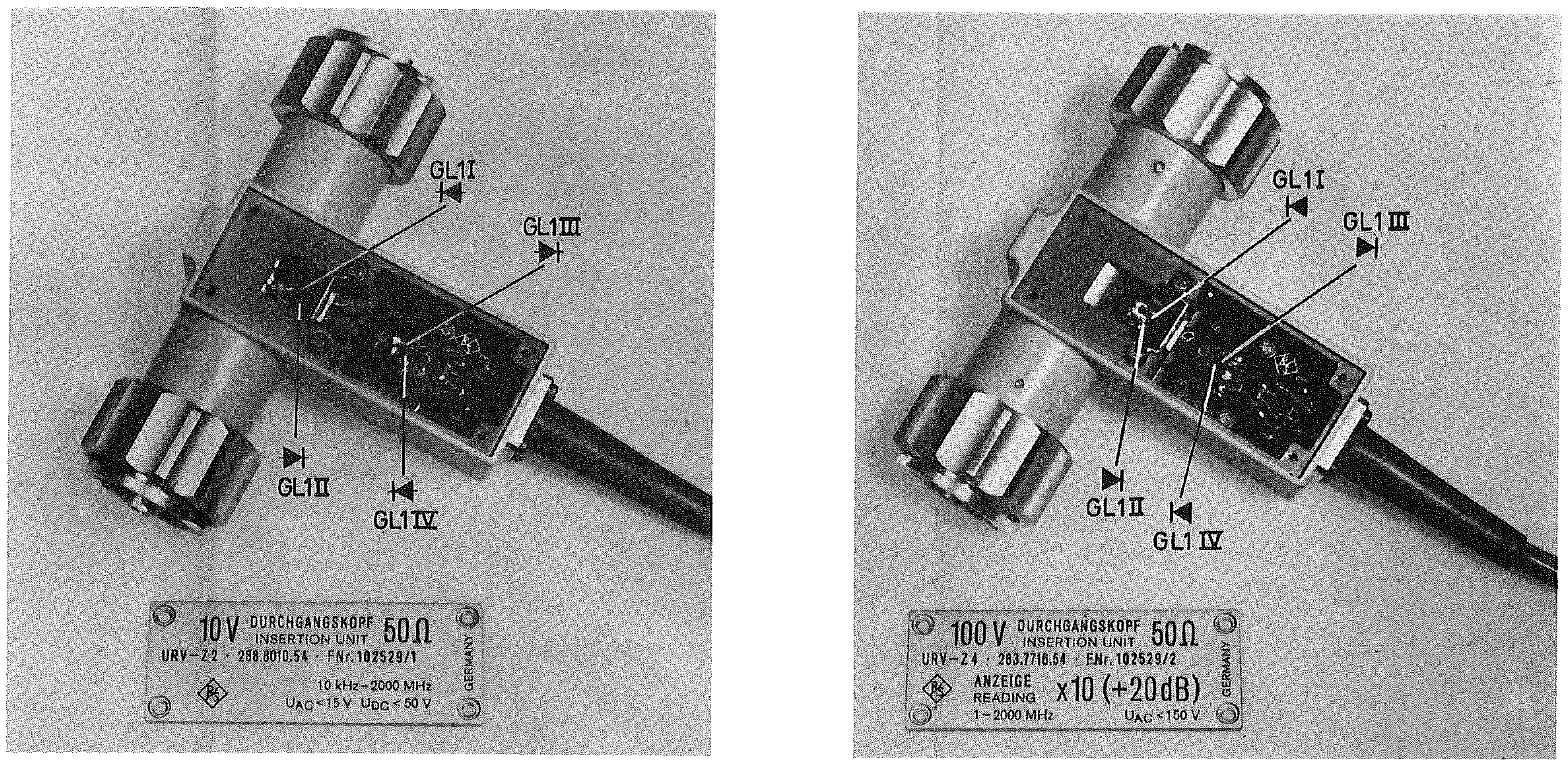


Bild 10 Durchgangsköpfe; Lage der Dioden

Fig. 10 Insertion units; location of diodes