144MHz FM TRANSCEIVER

TM-241A/E

SERVICE MANUAL

REVISED

KENWOOD

B51-8059-10(N)1177

This service manual is the same as the service manual (B51-8059-00) for TM-241A/E (TM-241A : K,P,M,M2 TM-241E : E,E2) destinations except that this manual contains new items for (TM-241A : M3,X,K2,P2 TM-241E : E9,EM) destinations.
Use it together with the previous service manual (B51-8059-00).

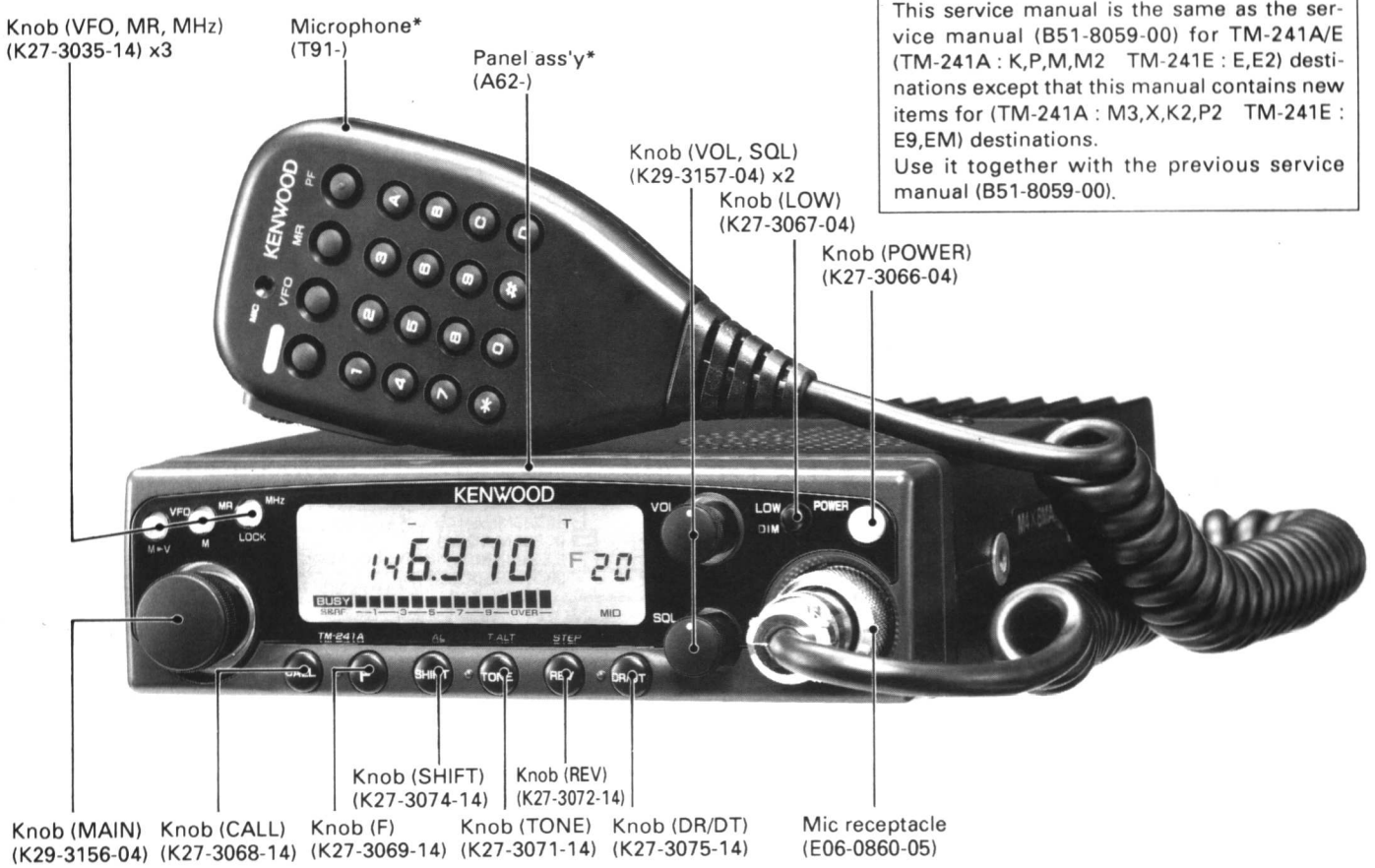

Photo is TM-241A.

*** Refer to parts list on page 15.**

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CIRCUIT DESCRIPTION

Circuit Configuration By Frequency

The TM-241A/E incorporates a PLL synthesizer which uses a digital VFO to allow any channel step of 5, 10, 12.5, 15, 20, or 25kHz to be selected (See Figure 1).

The receiving system utilizes double-conversion techniques. That is, an incoming signal is mixed down to the 1st intermediate frequency (IF) of 10.7MHz (K,P,X,M,M2,M3,E,E2,E9,EM), 30.825MHz (K2,P2), using a 1st local oscillator frequency of from 133.300 to 135.295MHz (E,E9,EM), 133.300 to 137.295MHz (M), 125.300 to 163.295MHz (K,P,X,M2,M3,E2), 105.175 to 166.820MHz (K2,P2). The 1st IF signal is then mixed with the 2nd local oscillator frequency of 10.245MHz (K,P,X,M,M2,M3,E,E2,E9,EM), 30.37MHz (K2,P2) to generate the 2nd IF of 455kHz.

The transmitting system consists of a PLL circuit which allows direct modulation and direct frequency division. Signals from the PLL circuit are amplified by a linear amplifier for transmission.

	TM-241A				TM-241E	
	K,P,X	K2,P2	M	M2,M3	E,E9,EM	E2
TX-RX UNIT (X57-369X-XX)	0-11	0-12	0-21	0-22	2-71	2-72

Table 1

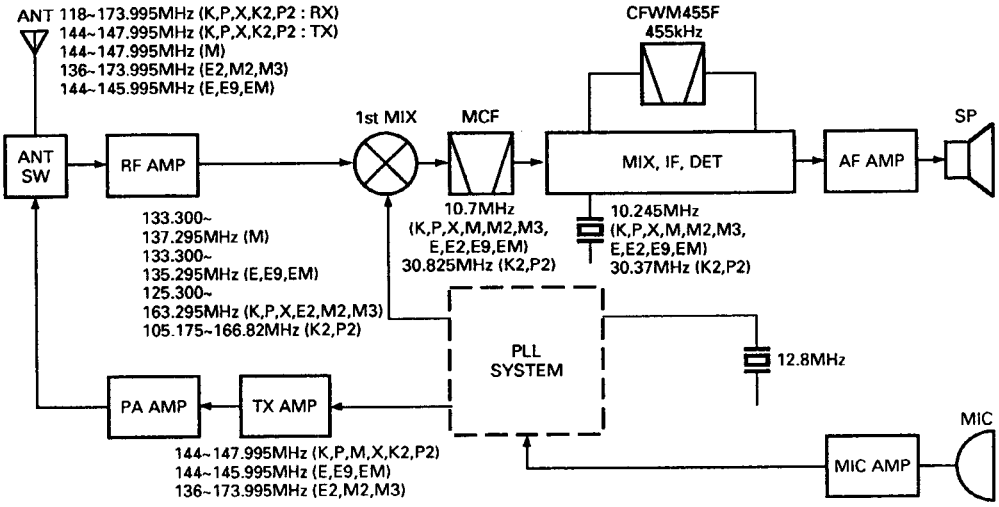


Fig. 1 Frequency configuration

Receiving System

- **Overview**

Incoming signals from the antenna pass through a low-pass filter in the final block of the transmitter system, and are switched to the front-end of the receiver system via a receive/transmit switching diode.

The signals are then passed through an antenna matching coil, where the high-frequency components are amplified by a GaAs FET. The signals are then fed into a three-stage band-pass filter that uses vari-cap tuning to reject unwanted signal components, and is fed to the 1st mixer. The 1st mixer uses the N-channel MOS FET that are used in the RF stage to obtain better two-signal characteristics. The 1st mixer mixes the signal with the 1st local oscillator frequency and converts it to the 1st IF (10.7MHz : K,P,X,M,M2,M3, E,E2,E9,EM, 30.825MHz : K2,P2). The signal then passes through two monolithic crystal filters (MCFs) to remove unnecessary near-by frequency components.

The signal from the MCFs is used as the 1st IF signal.

The 1st IF signal is amplified and fed into IC1 (KCD04) in the FM IF HIC. The IF signal is then mixed with the 2nd local oscillator frequency of 10.245MHz (K,P,X,M,M2,M3,E,E2,E9,EM), 30.37MHz (K2,P2) to generate the 2nd IF of 455kHz. The 455kHz signal is then passed through a six element ceramic filter (CFWM455F), and fed back into IC1 for additional amplification. The output signal from the IC1 is then fed into a power amplifier via the audio volume control for application to the speaker.

- **S-meter circuit**

S-meter control voltage from IC1 (KCD04) in the FM IF HIC is fed into the control unit. The CPU converters the voltage from an analog to digital signal in order to operate the LCD bar meter.

CIRCUIT DESCRIPTION

Item	Rating
Nominal center frequency (fo)	10.7MHz
Pass bandwidth	±7.5kHz or less at 3dB
Attenuation bandwidth	±25kHz or less at 40dB ±45kHz or less at 60dB
Ripple	1.0dB or less
Insertion loss	1.5dB or less
Guaranteed attenuation	70dB or more within ±1MHz Spurious 40dB or more at fo ~ fo+500kHz 80dB or more at fo – (900~920kHz)
Terminating impedance	3kΩ / 0pF

Table 2 MCF (L71-0228-15) TX-RX unit XF1 : K,P,M,M2,M3,X,E,E2,E9,EM

Item	Rating
Nominal center frequency (fo)	30.825MHz
Pass bandwidth	±7.5kHz or less at 3dB
Attenuation bandwidth	±28kHz or less at 40dB
Ripple	1.5dB or less
Insertion loss	3.0dB or less
Guaranteed attenuation	60dB or more within ±1MHz Spurious : 40dB or more
Terminating impedance	1.4kΩ / 1pF

Table 3 MCF (L71-0270-05) TX-RX unit XF1 : K2,P2

Item	Rating
Nominal center frequency	455kHz ± 1kHz
6dB bandwidth	±6kHz or more (from 455kHz)
50dB bandwidth	±12.5kHz or less (from 455kHz)
Ripple	3dB or less (within ±4kHz of 455kHz)
Insertion loss	6dB or less
Guaranteed attenuation	35dB or more (within ±100kHz of 455kHz)
I/O matching impedance	2.0kΩ

Table 4 Ceramic filter CFWM455F (L72-0372-05) TX-RX unit CF1

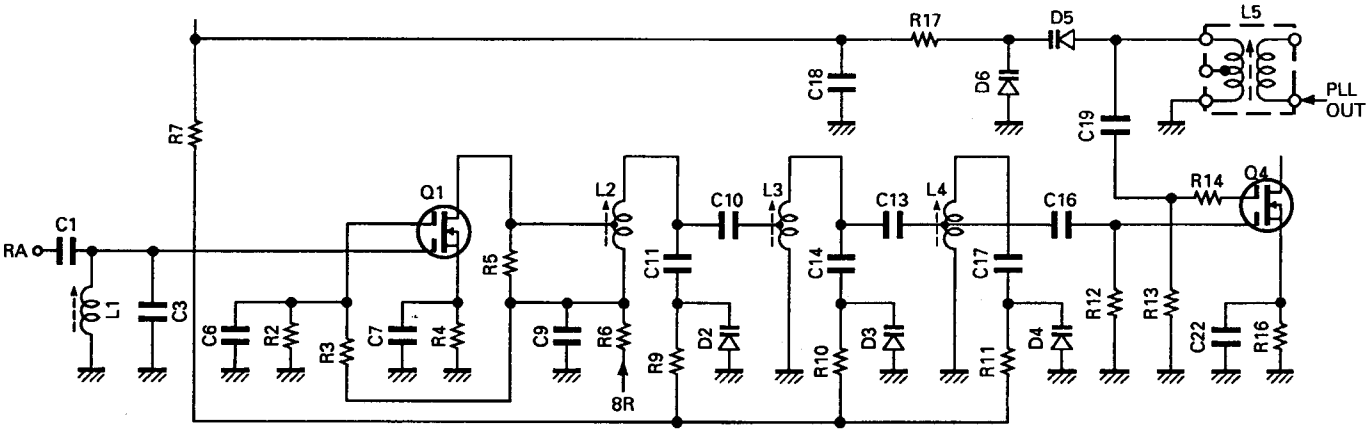


Fig. 2 Front-end section (vari-cap tuning)

CIRCUIT DESCRIPTION

Transmitting System

- **Overview**

The transmitter produces the target frequency thru the use of direct FM-modulation via a varactor diode.

- **Modulation circuit**

Audio signals from the microphone are fed into the mic amplifier unit for amplification by the 1st transistor amplifier, and then into two operational amplifiers. The operational amplifiers form a splatter filter for pre-emphasis, amplification, limiting, and removal of unnecessary high-frequency components.

The FM modulation circuit directly FM-modulates the VCO signals, using a varactor diode.

- **Pre-amplifier stage circuit**

Signals from the VCO are applied to the drive HIC IC8 (KCB05). The amplifier always operates in a linear mode so that signals can be amplified without degradation. Additionally, the amplifier is designed to cover a wide range of frequencies and can produce stable output without adjustment. The APC (Automatic Power Control) controls collector voltage from the last stage of the pre-amplifier.

- **Power amplifier circuit**

The drive signal is amplified to the required level by the power module. The TM-241A/E uses a large heat sink for efficient heat dissipation.

- **APC circuit**

The APC circuit for automatic transmit output control detects part of the power module output, and amplifies it to provide a control voltage for output control. The output control voltage is in inverse proportion to the output from the power module, so it is maintained at the same level.

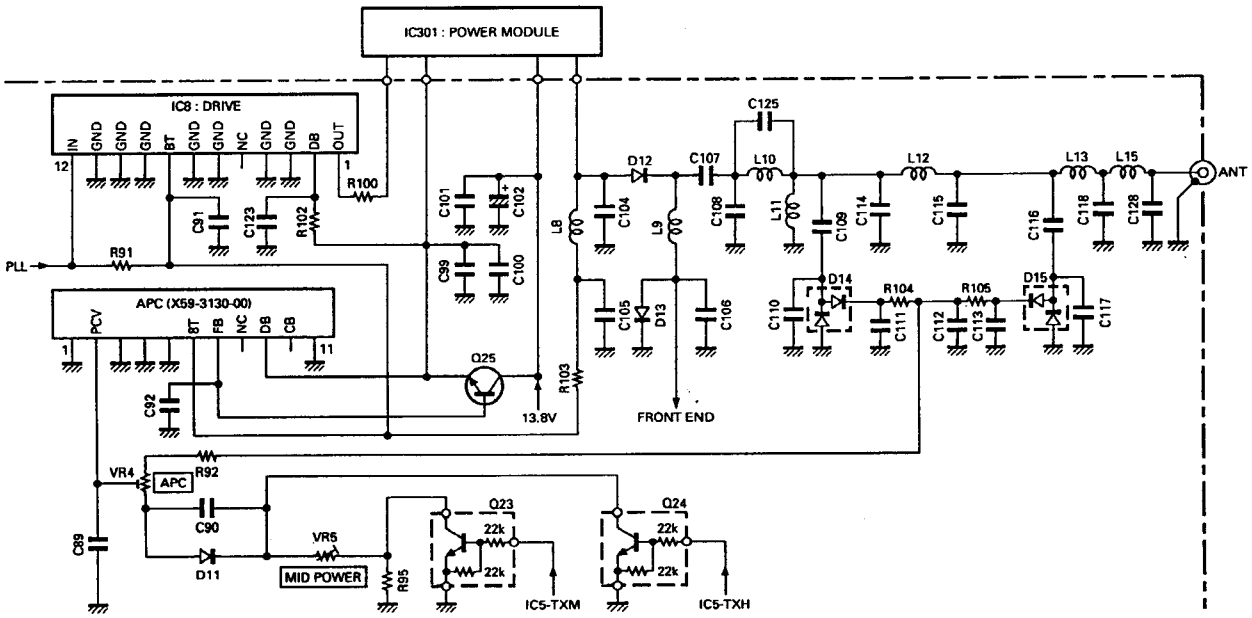


Fig. 3 Pre-amplifier stage, power amplifier, and APC circuits

(Tc = 25°C)

Item	Symbol	Condition	Rating	Unit
Operating voltage	Vcc		16	V
Control voltage	VCON		16	V
Current consumption	IT		14	A
Input power	Pi		600	mW
Output power	Po	12.5V < Vcc ≤ 16V, VCON ≤ 12.5V Pi = 0~500mW, ZG = ZL = 50Ω	65	W
Operating case temperature	Tc(opr)		-30~+100	°C
Storage temperature	Tstg		-40~+110	°C

Table 5 Power module S-AV17 maximum ratings (IC301)

CIRCUIT DESCRIPTION

PLL Synthesizer Unit (K,P,X,M,M2,M3,E,E2,E9,EM)

Figure 4-1 is the PLL and VCO block diagram. In the TM-241A/E, the PLL system is implemented as a sub-unit which is divided into the upper VCO and lower PLL blocks. The sub-unit is shielded to prevent external interference.

There are two reference frequencies, 6.25kHz and 5kHz, available to allow 5, 10, 12.5, 15, or 25kHz-step operation. The 6.25kHz is obtained by dividing the reference oscillator frequency of 12.8MHz by 2048, and the 5kHz is obtained by dividing it by 2560. The VCO directly generates the dial frequency. This dial frequency is amplified once and then fed into a pulse swallow-type PLL IC for frequency division and phase comparison, in order to lock the frequency.

The PLL system is locked without switching between transmit mode and receive mode. By using a signal ("H" in transmit mode) from pin 11 of the PLL IC (M54959FP), the LPF is deactivated-activated by Q52 and Q53 only for the moment when the TM-241A/E enters transmit mode. This helps produce lock more rapidly than previous methods.

In 144MHz mode, fvco (RX) is calculated by the following formula;

$fvco = (144 - 10.7) = \{(n \times 128) + A\} \times fosc \div R$

where,

- fvco : VCO output frequency
- n : Binary value of the 10-bit programmable counter
- A : Binary value of the 7-bit programmable counter
- fosc : 12.8MHz reference frequency
- R : Binary value of the 14-bit programmable counter
  2560 (5, 10, 15, 20, or 25kHz step mode)
  2048 (12.5kHz step mode)

In 5, 10, 15, 20, or 25kHz step mode,
n = 208 and A = 36.
Therefore, fvco is calculated as follows;

$fvco = \{(208 \times 128) + 36\} \times 12800 \div 2560$
$= (26624 + 36) \times 5$
$= 133300 = 133.300MHz$

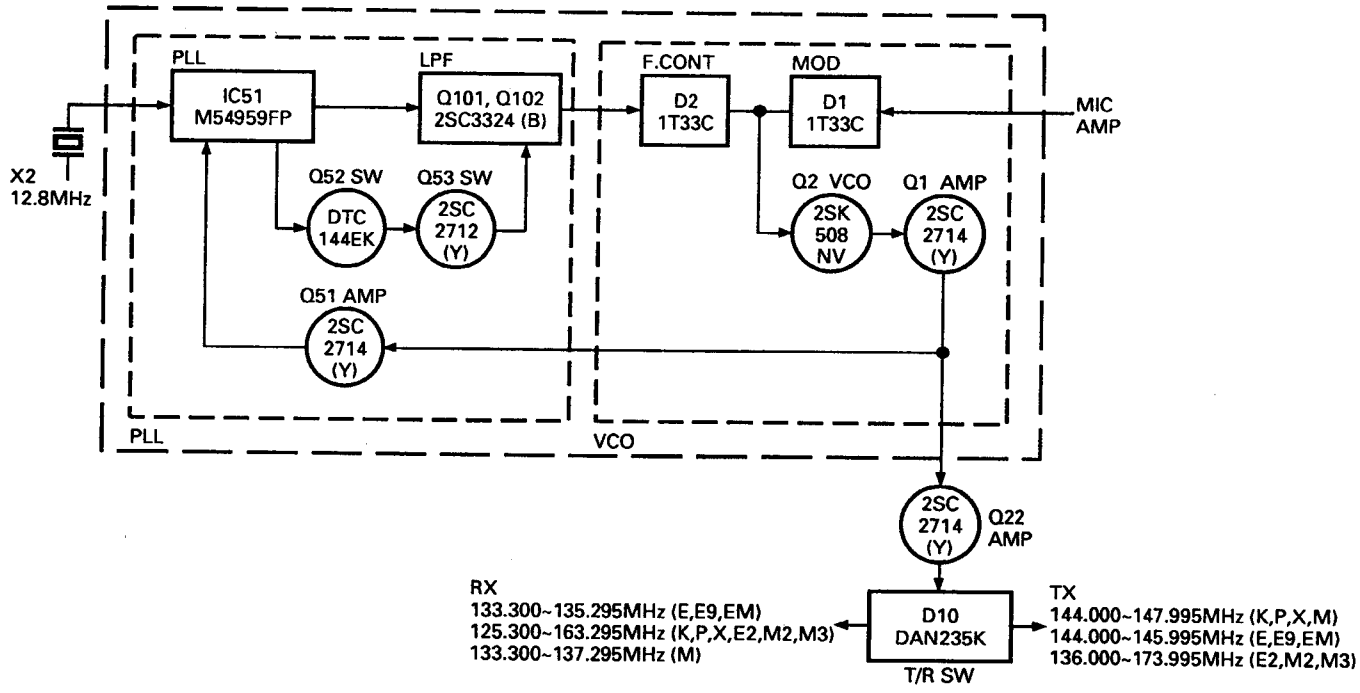


Fig. 4-1 PLL block diagram (K,P,X,M,M2,M3,E,E2,E9,EM)

CIRCUIT DESCRIPTION

PLL Synthesizer Unit (K2,P2)

Figure 4-2 is the PLL and VCO block diagram. In the TM-241A/E, the PLL system is implemented as a sub-unit which is divided into the upper VCO and lower PLL blocks. The sub-unit is shielded to prevent external interference.

There are two reference frequencies, 6.25kHz and 5kHz, available to allow 5, 10, 12.5, 15, or 25kHz-step operation. The 6.25kHz is obtained by dividing the reference oscillator frequency of 12.8MHz by 2048, and the 5kHz is obtained by dividing it by 2560. The VCO directly generates the dial frequency. This dial frequency is amplified once and then fed into a pulse swallow-type PLL IC for frequency division and phase comparison, in order to lock the frequency.

The PLL system has two VCOs, one for transmission and one for reception. Using a signal ("H" in transmit mode) from pin 10 of the PLL IC (M54959FP), the LPF is deactivated by Q105 only for the instant when the TM-241A/E enters transmit mode. This helps produce a more rapid PLL lock-up.

In 144MHz mode, fvco (RX) is calculated by the following formula;

$fvco = (144 - 30.825) = \{(n \times 128) + A\} \times fosc \div R$

where,

- fvco : VCO output frequency
- n : Binary value of the 10-bit programmable counter
- A : Binary value of the 7-bit programmable counter
- fosc : 12.8MHz reference frequency
- R : Binary value of the 14-bit programmable counter
  2560 (5, 10, 15, 20, or 25kHz step mode)
  2048 (12.5kHz step mode)

In 5, 10, 15, 20, or 25kHz step mode,
n = 176 and A = 107.
Therefore, fvco is calculated as follows;

$fvco = \{(176 \times 128) + 107\} \times 12800 \div 2560$
$= (22528 + 107) \times 5$
$= 113175 = 113.175MHz$

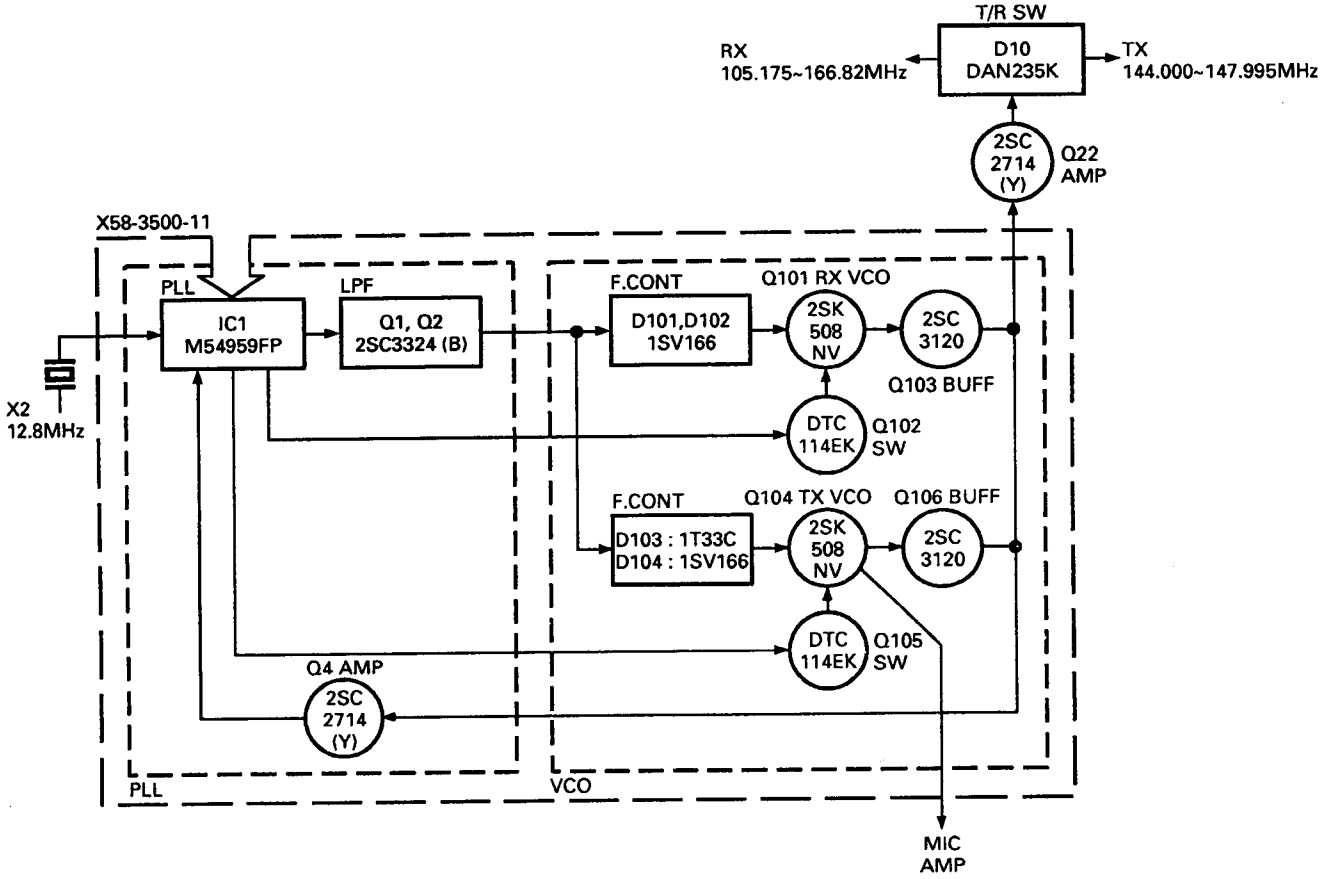


Fig. 4-2 PLL block diagram (K2,P2)

CIRCUIT DESCRIPTION

- **8T (8V in transmit mode) and unlock circuits**

In receive mode, the base of Q17 has 0.7V. As a result, Q17 is on, and Q16 and Q14 are off, and the collector of Q14 (8T) provides no voltage.

The CPU outputs serial data to the shift register IC5 when the PTT switch is depressed. As a result, pin 8 of IC5 becomes "L", turning Q17 off, and Q16 and Q14 on. The 8T line is therefore supplied with 8V.

The unlock circuit operates only in transmit mode. Q18 is a PLL unlocking switching transistor. Usually, the base of Q18 is supplied with 0V ("L"), and the collector is supplied with 8V ("H").

When the PLL is unlocked, the base of Q18 is supplied with 0.7V, turning Q18 on. As a result, the collector of Q18 becomes "L" (0V). This turns Q16 off and the collector of Q14 becomes 8V, turning it off. Therefore, when the PLL is unlocked, Q14 is off removing bias voltage from the 8T line. Without the 8T voltage no transmit signal is generated.

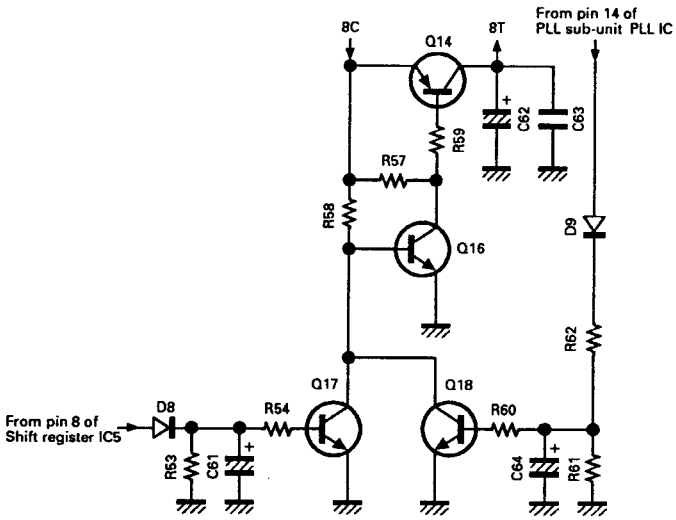


Fig. 5 8T and unlock circuits

Digital Control Unit

- **Overview**

The digital control unit consists of a several keys, a rotary encoder input, a display, a reset circuit, a back-up circuit, and a tone output circuit. These circuits are controlled by a single microcomputer (CPU).

- **Key and rotary encoder input circuits**

The keys on the panel are arranged in matrix. Key input is fed into the CPU, using a key scan technique. Output from the rotary encoder is fed directly into the CPU.

- **Microphone key input circuit**

The UP, DOWN, and other function keys of the microphone are directly connected to their corresponding analog input pins of the CPU. Each of the functions is activated by a voltage generated when the corresponding key is pressed.

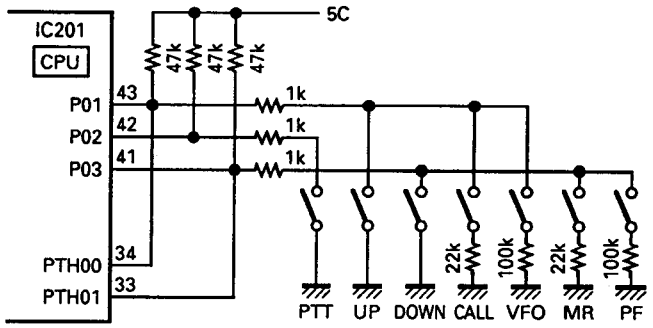


Fig. 6 Microphone key input circuit

- **Reset and back-up circuits**

When the TM-241A/E power is turned on, the reset circuit sends a "L" level pulse to the RESET pin of the CPU for approx. 3ms. This initiates the power-on reset sequence.

When the TM-241A/E power is turned off, the back-up circuit detects a voltage drop in the 5C line and sets CPU INT4 to a "H" level. This causes the CPU to enter a back-up state.

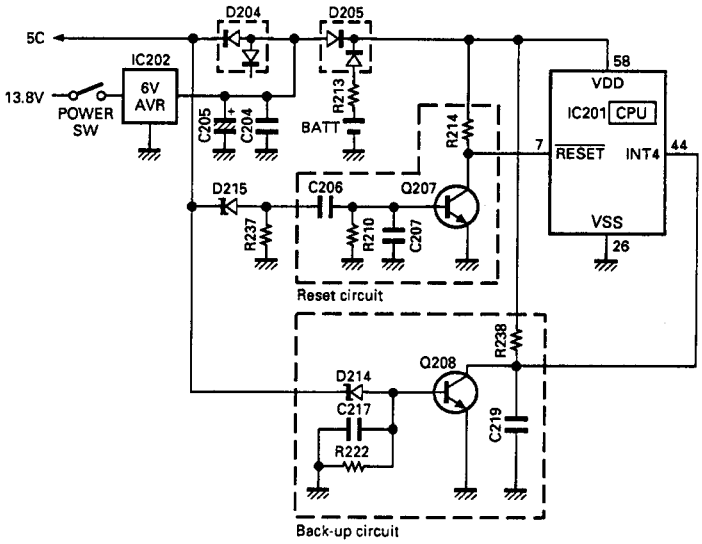


Fig. 7 Reset and back-up circuits

CIRCUIT DESCRIPTION

- **Display circuit**

The display circuit is contained in the LCD assembly. It consists of a LCD driver, its peripheral circuits, and an LCD. The LCD is dynamically operated at a 50% duty cycle. The LCD driver receives LCD data from P33, P140, and P141 of the CPU.

- **Dimmer circuit**

The lamp circuit generates a constant voltage of about 8.8V with SB, Q205, and D202. The lamp circuit resistance is changed by turning Q203 and Q204 on and off to control the dimmer. If the lamp is shorted, Q206 decreases the Q205 V_{BE} to prevent an over-current from flowing through Q205.

Brightness	Bright → Dark			
	1	2	3	4
P50	H	L	H	L
P51	H	H	L	L

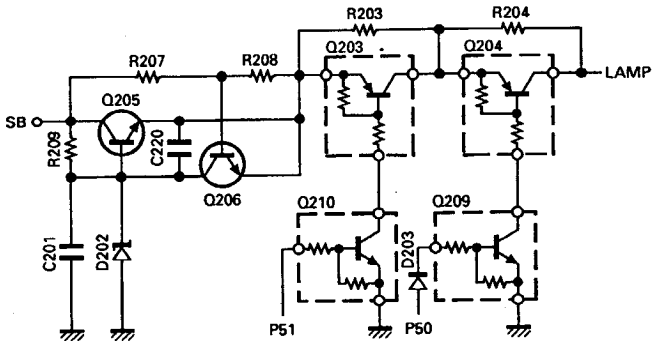


Fig. 8 Dimmer circuit

- **Shift register circuit**

The shift register circuit consists of IC5 (TC9174F). The IC5 receives serial data from the microcomputer to perform the controls listed below.

Pin No.	Pin name	Function
1	GND	
2	B1	Usually "H".
3	B2	Open.
4	CE	Electronic volume select. "H" when electronic volume selected, "L" when panel volume selected or interface connected.
5	VOLD	Electronic volume down. "L" when DOWN key on.
6	VOLU	Electronic volume up. "L" when UP key on.
7	MUTE	AF mute. "H" when TX mode, AL 1ch receive mode, CTCSS, T. ALT, or squelch is on.
8	T/R	Transmit/receive select. "H" in RX mode, "L" in TX mode.
9	TXM	TX power select. "H" in HI or MID mode, "L" in LOW mode.
10	TXH	TX power select. "H" in HI mode, "L" in MID or LOW mode.
11	–	Open.
12	–	Open.
13	DATA	Serial data input.
14	CLOCK	Clock input.
15	EN	Enable input.
16	V_{DD}	

Table 6

- **Tone output circuit**

R246 (ladder resisitor) receives signals from P40 to P43 and P52 to P53 of the CPU and converts them from digital to analog to produce 38 different waveforms from 67.0Hz to 250.3Hz. Figure 9 shows the internal configuration of R246.

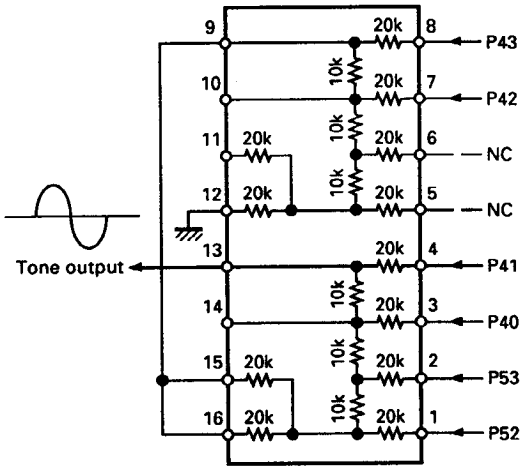


Fig. 9 Internal configuration of ladder resistor (TX-RX unit B/2 R246)

CIRCUIT DESCRIPTION

- **PLL data output**

PLL data is available from P21 (CK), P22 (DT), and P23 (EP1) of the CPU. Figure 10 is a timing chart for PLL data transfer, and Figure 11 shows the format of PLL data.

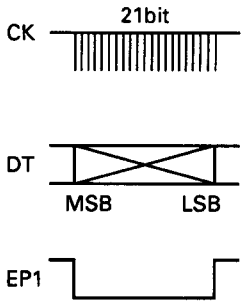
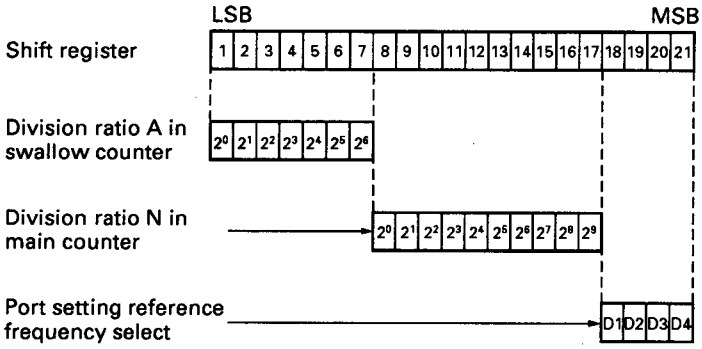


Fig. 10 Timing chart for PLL data transfer



The 21-bit data is made up of the following;

1. Division ratio data A and N (17 bits)

F (display – 10.7MHz or 30.825MHz in RX mode)

={(N x 128) + A} x 12.8MHz ÷ ref

N : Division ratio set in 10-bit main counter (binary)

A : Division ratio set in 7-bit swallow counter (binary)

2. Reference frequency (ref) select (2 bits)

Data		Phase reference frequency	
D1	D2		
L	L	5kHz	5, 10, 15, 20, 25kHz step mode
H	L	6.25kHz	12.5kHz step mode

3. Switch select (2 bits)

Data		Output port		
D3	D4	SW1	SW2	
L	H	L	H	RX mode
H	L	H	L	TX mode

Fig. 11 PLL data format

- **Input and output of CTCSS unit (option)**

The optional CTCSS unit receives data from P21, P22, and P73 of the CPU. Figure 12 is a timing chart for CTCSS data transfer, and Figure 13 shows the format of CTCSS data. When a tone form the CTCSS unit is detected, a "H" level signal is sent to TIO of the CPU, opening the squelch.

- **Input and output of the remote control unit (option)**

When the optional remote control unit is connected, a "H" level signal is applied to INT0 of the CPU, and the following pins have different functions;

P03 → S1 : Serial data input pin
P02 → S2 : Serial data output pin
P01 → SCK : Serial clock I/O pin

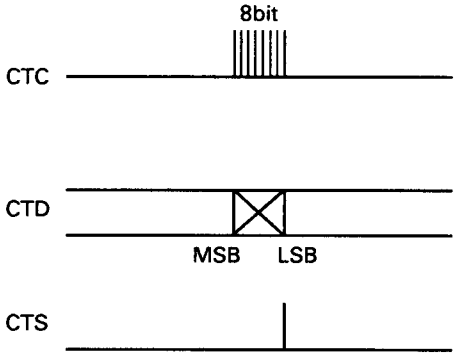


Fig. 12 Timing chart for CTCSS data transfer

Tone frequency select data for CTCSS unit

D1	D2	D3	D4	D5	D6
Example : 88.5Hz	L	H	L	H	H	H

Fig. 13 CTCSS data format

CIRCUIT DESCRIPTION

Pin No.	Pin name	I/O	Logic	Function
1, 2	P41, P40	O	–	D/A digital output (tone).
3, 4	P53, P52	O	–	D/A digital output (tone).
5, 6	P51, P50	O	–	Dimmer select.
7	$\overline{\text{RESET}}$	I	L	Reset input.
8, 9	X2, X1	–	–	4.194304MHz crystal oscillator.
10	P63	I	H	Function display.
11	P62	O	H	DRS remote control ST.
12	P61	O	–	DRS unit reset $\overline{\text{ACL}}$.
13	P60	I	H	DTMF signal detect.
14	P73	O	H	CTCSS unit enable output.
15	P72	O	H	Shift register enable output.
16	P71	O	H	DRS unit VOB output.
17	P70	O	H	DRS unit VOA output.
18	P83	O	H	DRS unit OE, DTSS EN output.
19	P82	O	H	DRS unit STBY output.
20	P81	O	L	DTSS DTSEL output, DRS unit $\overline{\text{WR}}$ output.
21	P80	O	L	DRS unit $\overline{\text{RD}}$ output.
22~25	P93~P90	O	H	DRS unit data output. D8/D3, D4/D2, D2/D1, D1/D0
26	Vss	–	–	GND.
27	P13	I	H	DRS unit connect check.
28, 29	INT2, INT1	I	–	Encoder input.
30	P10	I	H	Remote connect detect input.
31	PTH03	I	–	S-meter analog input.
32	PTH02	I	–	Not used (GND).
33	PTH01	I	–	Microphone DOWN/MR/PF input.
34	PTH00	I	–	Microphone UP/CALL/VFO input.
35	TI0	I	H	CTCSS unit DET input.
36	TI1	I	L	Not used (GND).
37	P23	O	L	PLL IC enable output.
38	P22	O	–	Serial data output.
39	P21	O	–	Serial clock output.
40	P20	O	–	Beeper output.
41	P03/SI	I/I	L/–	Serial data input. (KENWOOD BUS)
42	P02/SO	I/O	L/–	Serial data output. (KENWOOD BUS)
43	P01/$\overline{\text{SCK}}$	I/–	L/–	Serial clock I/O. (KENWOOD BUS).
44	INT4	I	H	Back-up detect input. Back-up : "H"
45	P123	I	L	CALL, VFO key and destination input.
46	P122	I	L	F, MR/M key and destination input.
47	P121	I	L	SHIFT, MHz key and destination input.
48	P120	I	L	TONE key and destination input.
49	P133	I	L	REV key and destination input.
50	P132	I	L	LOW, DRS/DTSS key and destination input.
51	P131	I	L	Not used (GND).
52	P130	I	L	Busy input.
53	P143	O	L	Squelch control.
54	P142	O	H	Power switch.
55	P141	O	–	LCD driver clock output.
56	P140	O	–	LCD driver data output.
57	NC	–	–	Not used (V_{DD}).
58	V_{DD}	–	–	Power supply pin.
59	P33	O	–	LCD driver enable output.
60	P32	O	L	Destination output.
61, 62	P31, P30	O	L	Key output.
63, 64	P43, P42	O	–	D/A digital output (tone).

Table 7 CPU : 75116GF-XXX-3BE terminal functions (TX-RX unit IC201)