PLESSEY
Semiconductors

SP8703

1GHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8703 is a divide by 128/9 programmable divider with a maximum specified operating frequency of 1GHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The output stage is CMOS compatible only, the 0 to 1 output edge giving best loop delay performance.

A unique 'power-down' feature is included to minimise power consumption.

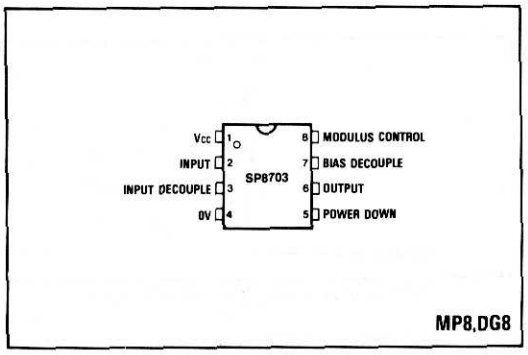


Fig.1 Pin connections - top view

FEATURES

- DC to 1GHz Operation
- -30° to +70°C Temperature Range
- Unique Power-Down Feature
- CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 30mA Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	6V
Storage temperature range	-30°C to +150°C
Max. junction temperature	+175°C
Max. clock I/P voltage	2.5V p-p

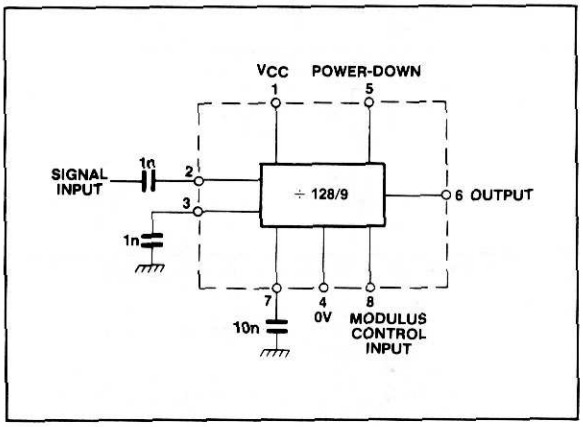


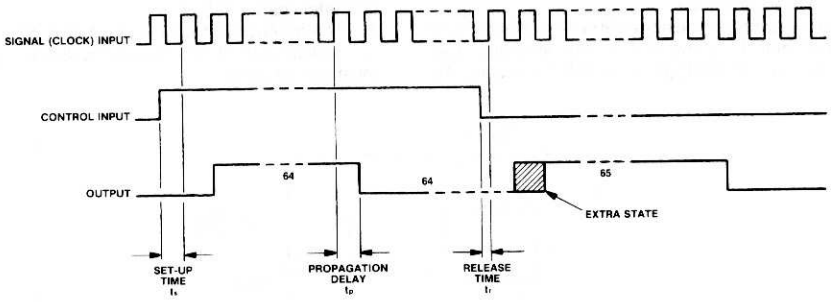
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +4.75V to 5.25V, T_{amb} = -30°C to +70°C

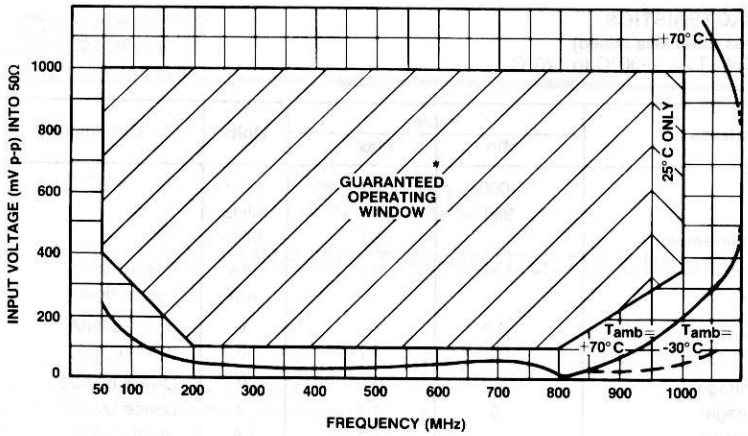
Characteristics	Value		Units	Conditions	Notes
	Min.	Max.			
Maximum frequency	1000		MHz	T_{amb} = 25°C	Note 1,2,4
Maximum frequency	950		MHz		Note 1,2,3
Minimum frequency (sinewave)		50	MHz		Note 1,2,3
Power supply current		40	mA	Power-up	Note 3
Power supply current		3	mA	Power-down	Note 3
Output high voltage	3.2	V_{CC}	V	IL = -0.2mA	Note 3
Output low voltage	0	1.7	V	IL = 0.2mA	Note 3
Control input high voltage	3.2	V_{CC}	V	Divide by 128	Note 3
Control input low voltage	0	1.7	V	Divide by 129	Note 3
Control input high current		50	μA	Input = V_{CC}	Note 3
Control input low current	-10		μA	Input = 0V	Note 3
Power-down high voltage	3.2	V_{CC}	V	Power-down	Note 3
Power-down low voltage	0	1.7	V	Power-up	Note 3
Power-down high current		10	μA	Input = V_{CC}	Note 3
Power-down low current	-2		μA	Input = 0V	Note 3
Clock to output delay		30	ns	CL = 10pF	Note 5
Set-up time		15	ns	CL = 10pF	Note 5
Release time		15	ns	CL = 10pF	Note 5

NOTES
1. See Fig.4 for guaranteed operating window.
2. See Fig.5 for input voltage measurement method.
3. Tested at 25°C and +70°C only.
4. Tested at 25°C only.
5. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷128 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷129 mode is obtained.

Fig.3 Timing diagram



*Tested as specified in table of Electrical Characteristics

Fig.4 Typical input characteristics

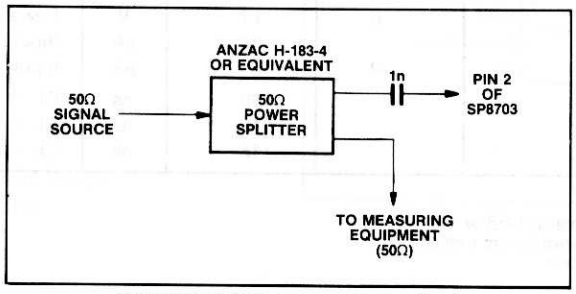


Fig.5 Input voltage measurement method

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/μs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.